IOP Publishing Journal of Physics D: Applied Physics
J. Phys. D: Appl. Phys. **40** (2007) 2754–2758 doi:10.1088/0022-3727/40/9/012

Fabrication and charging characteristics of MOS capacitor structure with metal nanocrystals embedded in gate oxide

Weihua Guan, Shibing Long, Ming Liu[1], Zhigang Li, Yuan Hu and Qi Liu

Laboratory of Nano-fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China

E-mail: liuming@ime.ac.cn

Received 8 February 2007, in final form 7 March 2007
Published 19 April 2007
Online at stacks.iop.org/JPhysD/40/2754

Abstract
Metal–oxide–semiconductor capacitor structure with metal nanocrystals embedded in the gate oxide for the application of nonvolatile memory (NVM) is fabricated. Optimal process parameters are investigated and Au nanocrystals are adopted in this paper. High-frequency capacitance versus voltage (C–V) and conductance versus voltage (G–V) measurements demonstrate the memory effect of the structure which is shown to originate from the confined states of metal nanocrystals. Capacitance versus time (C–t) measurement under a constant gate bias is executed to evaluate the retention performance and an exponential decaying trend is observed and discussed. It is found that with respect to semiconductor counterparts, Au nanocrystals can provide enhanced retention performance, which confirms the high capacity of Au nanocrystals for NVM applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Recently, nonvolatile memory (NVM) devices utilizing discrete nanocrystals (ncs) as floating gate have received considerable attention due to their excellent memory performance and high scalability. In nanocrystal floating gate memory devices, nanocrystals such as semiconductor [1, 2], metal [3], compound [4, 5] or hetero-nanocrystal [6] are embedded between the control oxide layer and the tunnelling oxide as charge storage nodes to replace the continuous floating gate layer used in conventional NVM. As a result, the devices can be less sensitive to local oxide defects. Thinner tunnelling oxide can be adopted without significant degradation in retention performance, the programming voltage can be reduced and the programming/erase (P/E) speed can be improved significantly. For compound materials and hetero-nanocrystals based memory, the somewhat complex fabrication process is economically unsuitable. For semiconductor nanocrystal (nc-Si and nc-Ge) memories, the relatively long retention times observed in the experiment are suggested to be related to the traps and defects inside or at the surface of nanocrystals [7, 8], which are sensitive to the thermal processes in device fabrication and therefore bringing obstacles for thermal budget in device integration. Among the research efforts to improve the overall performance of the nc memory, metal nanocrystal is proposed as an efficient way to prolong the charge retention time [9]. Since the availability of various metal work functions makes it easy to tune the depth of the potential well where the charges are stored, an asymmetrical barrier between the storage nodes and the substrate can be created, which makes it possible to form a small barrier for programming while a large barrier for retention and thus fast P/E speed and long retention time can be achieved simultaneously. In order to characterize the electrical properties of ncs at the nanometre scale, several groups [10–13] have applied the conductive atomic force microscopy (C-AFM) technique to probe the localized charging and discharging behaviour in

[1] Author to whom any correspondence should be addressed.

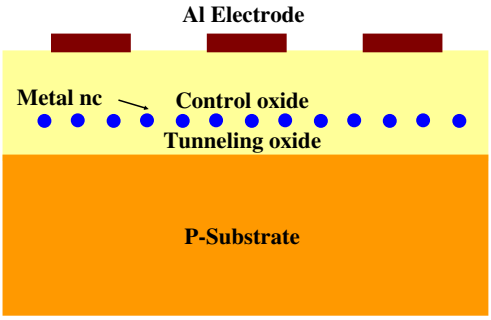

Figure 1. Schematic cross-sectional structure of fabricated capacitor.

nc-Si. Although the C-AFM technique presents more detailed and microcosmic information about electrical properties of ncs as compared with the traditional capacitance versus voltage (C–V) technique, it calls for delicate experimental installation.

In this study, we investigate the feasibility of several metal nanocrystals (including Au, Ni and Co) embedded in the gate oxide of metal–oxide–semiconductor (MOS) capacitor structure for NVM application. Metal nanocrystals are formed by electron-beam evaporation combined with rapid thermal annealing (RTA) which is a self-assembling process. The electrical characteristics of a MOS capacitor structure containing gold nanocrystals (nc-Au) are studied by various electrical measurement methods.

2. Experiment details

Figure 1 shows the schematic cross-sectional structure of the MOS capacitor discussed in this paper. After chemically cleaning the (1 0 0) p-type silicon wafer (1–10 Ω cm), a 5 nm tunnelling SiO_2 layer is thermally grown in dry oxygen at 700 °C. A thin metal wetting layer is then deposited via e-beam evaporation with the deposition ramp of 0.3 Å s^{-1} and chamber pressure of 2.6 × 10^{-6} Torr. The thickness of the thin metal layer is monitored by a quartz crystal oscillator. RTA under a certain temperature is carried out in N_2 ambient to induce the formation of metal nanocrystals. After this step, the surface morphology of some samples is characterized by HITACHI S-4800 ultra-high resolution SEM. Then a layer of 25 nm SiO_2 as control oxide is deposited by plasma enhanced chemical vapour deposition (PECVD) with the furnace temperature at 280 °C. After that, 200 nm aluminium top electrodes with 10^{-3} cm^2 area are evaporated using a circle-shaped shadow mask. Control samples without any metal nanocrystals are simultaneously fabricated with the same process. The charge storage characteristic of the metal nanocrystals embedded in silicon oxides is analysed by high-frequency (1 MHz) capacitance versus voltage (C–V) and conductance versus voltage (G–V) measurements with a Keithley 4200 semiconductor characterization system and a 590 C–V analyser at room temperature. The charge retention performance is also studied through the transient capacitance (C–t) testing techniques.

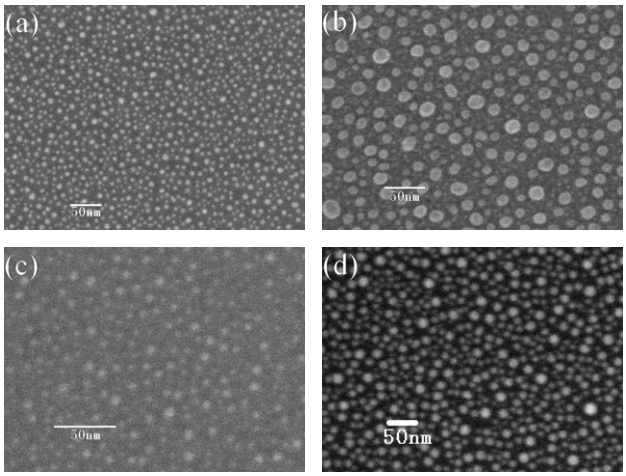

Figure 2. High resolution SEM planar images of the metal ncs formed under different process parameters: (*a*) Au with an initial thickness of 1.5 nm and annealed at 600 °C. (*b*) Ni with an initial thickness of 1 nm and annealed at 800 °C. (*c*) Ni with an initial thickness of 2 nm and annealed at 800 °C. (*d*) Ni with an initial thickness of 2 nm (note that the Ni thin film under this condition is fabricated through sputtering, not e-beam evaporation) and annealed at 800 °C.

Table 1. Impact of the fabrication process on the formation of metal nanocrystals.

Metal material	Initial thickness (nm)	Annealing temperature (°C)	Size range (nm)	Density (cm^{-2})
Au [a]	1.5	600	6–7	4×10^{11}
Co [b]	1.5	700	7–14	1.6×10^{11}
Ni	1	800	8–20	2×10^{11}
Ni	2	800	4–8	2.5×10^{11}
Ni [c]	2	800	10–20	1.6×10^{11}

[a] The condition we used to fabricate the MOS capacitor structure.
[b] SEM image not shown here.
[c] This Ni wetting layer is fabricated through sputtering not e-beam evaporation.

3. Result and discussion

In our experiment, three kinds of metals (Au, Ni and Co) are utilized and it is found that the initial metal wetting layer thickness and the post-RTA temperature have a significant impact on the quality of the nanocrystals. With a thicker initial wetting layer, it is hard to form discrete ncs under any post-RTA condition. A thickness below 2 nm can induce the formation of ncs, even without the post-RTA processing. With the same thickness for a given metal material, although the RTA process facilitates the nucleation of the metal wetting layer, an over high RTA temperature deteriorates the nc quality. As a result, a moderate RTA temperature is favoured for a given metal material. Figure 2 shows part of the scanning electron microscope (SEM) planar images of the metal nanocrystals formed under different process parameters and the results are summarized in table 1. It is found that an Au wetting layer with an initial thickness of 1.5 nm annealed at 600 °C for 30 s produces nanocrystals with the most satisfying qualities such as uniformity, small size and relatively high density. The high resolution image of the nc-Au (figure 2(*a*)) shows that

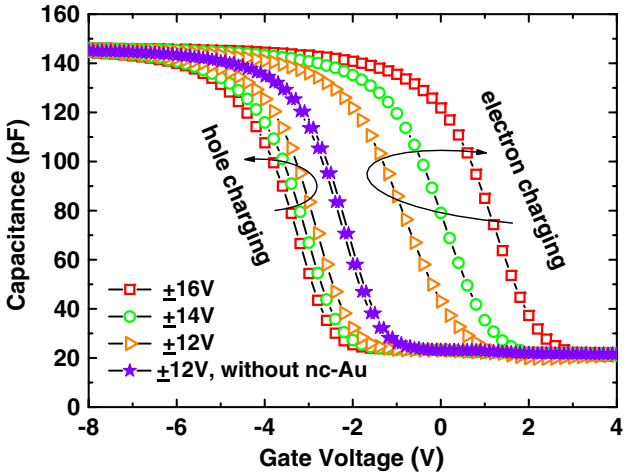

Figure 3. Typical high-frequency C–V hysteresis under different bi-direction scan voltage ranges.

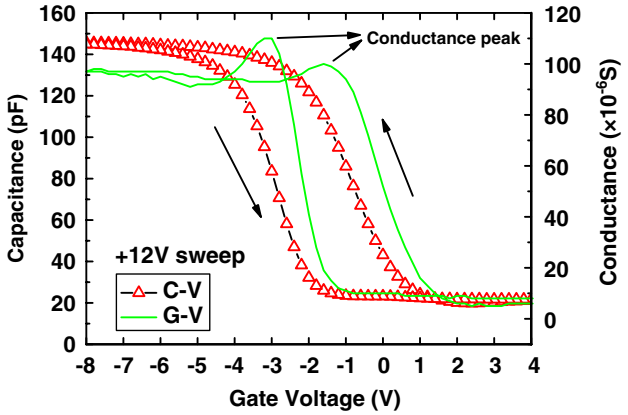

Figure 4. High-frequency C–V and G–V curves measured under ±12 V back and forth sweep.

their average diameter is about 6–7 nm and that their shape is mainly spherical. The nanocrystals are separated well from one another and distributed uniformly. No aggregation of the nc-Au is observed. The estimated density of the dispersed nc-Au is about 4×10^{11} cm^{-2}. As a result, e-beam evaporation combined with RTA is an effective method to form high quality gold nanocrystal arrays. Unless otherwise mentioned, the following discussion concerning the electrical performances is restricted to the MOS capacitor with nc-Au embedded.

The charging characteristics of Au nanocrystals embedded in silicon oxide analysed by 1 MHz C–V measurement at room temperature (300 K) are shown in figure 3. The dc gate bias is swept from a negative voltage to a positive voltage and then returns to the initial value. As a result, the quasi-MOS structure is swept between accumulation and inversion regions. As shown in figure 3, the C–V curve of the control sample without nc-Au (stars) exhibits negligible hysteresis which is similar to the ordinary MOS high-frequency C–V curve. A conspicuous counterclockwise hysteresis, however, is observed for the MOS capacitor with nc-Au embedded when the gate bias is swept back and forth. Note that the centre of the hysteresis curve is around −2 V, which, in ideal conditions, should be near 0 V. This deviation may be caused by the excessive immobile positive charges existing in the oxide layer and the work function difference between the Al electrode and silicon [14]. The observed counterclockwise hysteresis is attributed to the charging and discharging process in the MOS capacitor structure. When a positive bias is applied, electrons are injected from the inversion layer of the Si substrate into the gate oxide matrix. When a positive bias is applied, electrons are ejected from the MOS gate matrix into the Si substrate (equivalent to hole injection). As indicated in figure 3, the left three branches represent hole charging states while the right three branches represent electron charging states and it is obvious that electron charging is the dominant mechanism in our samples due to the larger shift of the flat-band voltage ($V_{\rm fb}$) in the right branches than the left branches. The injection of electrons or holes leads to $V_{\rm fb}$ shift (so-called memory window), the magnitude of which is found to be dependent on the voltage sweeping range. For example, the memory window is about 4.5 V for a ±16 V sweep, 3 V for a ±14 V sweep and 2 V for a ±12 V sweep, respectively. Generally, the memory window is found to increase with increasing gate bias, indicating more charges are injected. According to the formula given by Tiwari *et al* [1], it is able to approximately quantify the average amount of electrons per nanocrystal after programming. For instance, the voltage shift of 2 V at a ±12 V sweep corresponds to a charge density of 1.6×10^{12} cm^{-2}. Considering the density of ncs in gate oxide as 4×10^{11} cm^{-2}, it can be estimated that there are about four electrons per nanocrystal on average, which suggests that it is a few-electron device.

Up to now, though several groups have carried out experiments to investigate the charge storage mechanism for nanocrystal memories [7, 15–17], discrepancies exist. For example, Shi *et al* [7] and Koh *et al* [8] suggest that the traps internal to or on the surface of nc-Si (or nc-Ge) have a strong influence on charge storage behaviour. Huang *et al* showed that in their samples, neither an interface defect nor a deep defect is dominant for the charging and discharging processes, using C–V and G–V testing techniques [15]. As we can easily tell, there are four main charge storage locations in MOS capacitors with nanocrystals embedded: (1) the interface states between the SiO_2 and the substrate, (2) the traps or defects distributed in the SiO_2 layer, (3) nanocrystal confined states and (4) the interface states between the nanocrystals and the surrounding SiO_2 matrix [16]. Since the control sample has the same processing flow with the sample containing nc-Au, the absence of hysteresis for the control sample can exclude the possibility that the charging effect for a MOS capacitor containing nc-Au originates from the interface states between the silicon substrate and SiO_2 as well as the traps or defects inside the SiO_2 layer. The charging effect is then naturally attributed to the existence of metal nanocrystals, either in the confined states or in the interface states with surrounding SiO_2. This conclusion is also supported by the high-frequency G–V measurement under a ±12 V bi-direction sweep, as shown in figure 4. The position of the conductance peak close to $V_{\rm fb}$ in either sweep direction confirms the observed hysteresis and peak shifts should be both related to metal ncs [15]. However, it is worth noting that using such a comparison between the samples with and without ncs, it is still impossible to further clarify whether the charges are stored in the nanocrystal or at the interface state with the oxide. The most recent experiment

done by Liu *et al* suggests that the nanocrystals, rather than the nc/SiO_2 interface, play the dominant role in the charging effect [17]. In our case, because of the huge number of electrons for Au nanocrystals (thus a high density of states), the effect of traps and defects can be ruled out as the dominant mechanism for charging behaviour [9]. Therefore, we can cautiously come to the conclusion that in the MOS capacitor with nc-Au embedded, the confined states of nc-Au are the predominant mechanism for electron charging.

In order to analyse the charge retention capacity of nc-Au embedded MOS capacitor structure, capacitance versus time (C–t) measurement under a fixed gate bias is performed. Figure 5 displays the normalized capacitance–time curve for the fabricated structure with nc-Au. The transient capacitance is measured after charging nc-Au by applying a +12 V gate bias for 5 s and then fixing the gate voltage to a constant negative bias (−1 V) around the flat-band voltage (−2 V in our case). As shown, after a period of time for negative bias stress, the capacitance of the MOS capacitor is reduced by some degree, which suggests that the electrical state of the MOS capacitor is altered. Since the higher capacitance corresponds to the electron charged state of the nc-Au and the lower capacitance corresponds to the electron discharged state, the diminishing trend of the C–t curve can be translated into the charge decaying behaviour of nc-Au. Note that the C–t plot displays obvious two-stage behaviour: the initial fast decaying stage and the subsequent slow decaying stage, which can be understood as follows: when the programming process is finished at time $t = 0$, the charge density in the ncs has its maximum value. The electrical field in the tunnelling dielectric is then the strongest. As a result, the discharging current is the largest and the charge loss rate is the fastest at the initial stage of the retention period. With electrons tunnelling out of ncs, the charge density as well as the electrical field decreases. Thus, the process of charge loss becomes slower and slower.

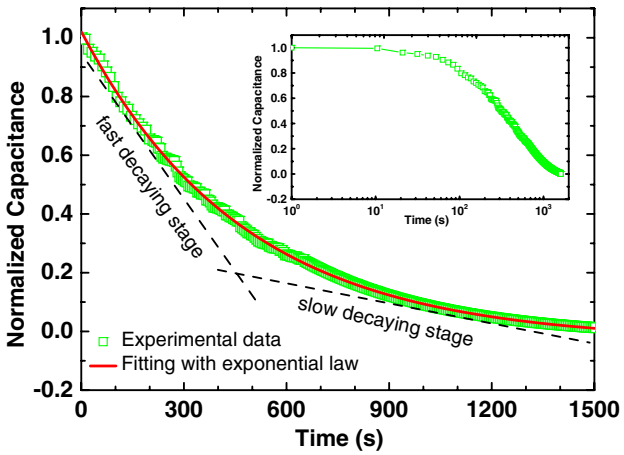

Figure 5. Normalized capacitance versus time (C–t discharging curves $(C(t) - C(\text{sat}))/(C(t = 0) - C(\text{sat}))$ for MOS capacitor structure with nc-Au embedded, $C(\text{sat})$ denotes the capacitance at the end of the test. It is performed after charging the MOS structure at 12 V for 5 s and under a gate stress voltage of −1 V. The inset shows the semi-logarithmic plot.

Another interesting phenomenon is that unlike the reported logarithmic decaying shape of the C–t curve [18, 19], which involves a variation of the tunnelling probability with time, the C–t curve under our testing conditions exhibits an exponential variation with time. As shown in figure 5, the experimental data fit the exponential function ($f(t) = \alpha \cdot \exp(-t/t_0) + \beta$) quite well. This suggests a constant tunnelling probability and thus a constant electric field in the oxide during the transient capacitance measurement. It can be understood as follows: according to Busseret *et al* [18], the electric field in the gate oxide comes from two components: one is the gate bias and the other is the stored charges in the nanocrystals. The effective field is the sum of them. In the reported C–t results [18, 19], they select the flat-band voltage (V_{fb}) as the gate stress bias and thus the field due to the gate voltage equals zero. As a result, the electric field in the oxide is only due to the stored charge in the nanocrystals. However, things are different in our case: the voltage we choose as the gate stress bias (−1 V) is not the flat-band voltage (−2 V) in our measurements. From the fact that the experimental C–t data fit the exponential function quite well, we can conclude that, under our test conditions, the gate bias plays a dominant role in determining the electric field in the gate oxide and the electric field due to the stored charge in ncs is negligible or not significant and thus the electric field in the oxide as well as the tunnelling probability is nearly constant during measurement which will result in the exponential decaying shape of the C–t curve [18].

When compared with the retention performance for the MOS capacitor with semiconductor nanocrystals embedded [8, 20], the retention time of nc-Au is greatly enhanced, as summarized in table 2, in which the retention time is defined as the time taken for the capacitance to decrease to 50% of the initial value and all the data are based on the same normalized methods: $(C(t) - C(\text{sat}))/(C(t = 0) - C(\text{sat}))$. All measurements are performed at room temperature. With comparable device parameters and more severe stress condition, the MOS capacitor with nc-Au embedded in this work shows prolonged retention time with respect to the semiconductor counterparts. This is consistent with the results reported by Lee and Kwong [21] and Zhao [22]. Therefore, the nc-Au based structure is promising for NVM applications.

Table 2. Comparison of the retention performance for MOS capacitors with metal and semiconductor nanocrystals embedded.

nc	nc size	Tunnelling barrier	Stress condition	Retention time (s)
Ge [8]	5.67 ± 1.31 nm	5 nm SiO_2	V_{fb}	90
Ge [20]	Unknown	5 nm SiO_2	V_{fb}	80
Au [This work]	6–7 nm	5 nm SiO_2	−1 V under V_{fb}	300

4. Conclusions

MOS capacitor structure employing metal nanocrystals as floating gate, prepared by e-beam evaporation combined with RTA, is fabricated for the application of NVM. The influence of the different process conditions on the formation and quality of the metal nanocrystals is investigated. Gold nanocrystals (nc-Au) with an average size of 6 nm and density of $4 \times 10^{11}\,\mathrm{cm}^{-2}$ are used to study the electrical characteristics of the MOS capacitor. The charging effect is identified through high-frequency (1 MHz) C–V and G–V measurements. The flat-band voltage shift found in the C–V curves is attributed to the electron injection from the inversion layer in the Si substrate to the Au nanocrystals through the tunnel oxide. The memory window increasing with the increase in the gate bias suggests that more electrons are stored. The transient capacitance measurement technique is used to evaluate the retention performance of MOS capacitor structure with nc-Au embedded in the gate oxide. The different appearance of the C–t curve between the reported results and our work is observed and discussed. The nc-Au with high work function (5.0 eV) shows enhanced charge retention time with respect to semiconductor nanocrystals, and thus the high potentiality of Au nanocrystals for NVM applications is confirmed.

Acknowledgments

This work is partly supported by the National Basic Research Program of China (973 Program) under Grant No 2006CB302706 and the National Natural Science Foundation of China under Grant No 90607022, 90401002, 60506005 and 60390071.

Reference

[1] Tiwari S, Rana F, Hanafi H, Hartsten A, Crabbe E F and Chan K 1996 *Appl. Phys. Lett.* **68** 1377–9

[2] Wu J H and Li P W 2007 *Semicond. Sci. Technol.* **22** S89–S92

[3] Yim S-S, Lee M-S, Kim K-S and Kima K-B 2006 *Appl. Phys. Lett.* **89** 093115

[4] Lin Y-H, Chien C-H, Lin C-T, Chang C-Y and Lei T-F 2005 *IEEE Electron Devices Lett.* **26** 154–6

[5] Chen J H, Yoo W J, Chan D S H and Tang L J 2005 *Appl. Phys. Lett.* **86** 073114

[6] Zhu Y, Li B, Liu J, Liu G F and Yarmoff J A 2006 *Appl. Phys. Lett.* **89** 233113

[7] Shi Y, Saito K, Ishikuro H and Hiramoto T 1998 *J. Appl. Phys.* **84** 2358–60

[8] Koh B H, Kan E W H, Chim W K, Choi W K, Antoniadis D A and Fitzgerald E A 2005 *J. Appl. Phys.* **97** 124305

[9] Liu Z, Lee C, Narayanan V, Pei G and Kan E C 2002 *IEEE Trans. Electron Devices* **49** 1606–13

[10] Boer E A, Bell L D, Brongersma M L, Atwater H A, Ostraat M L and Flagan R C 2001 *Appl. Phys. Lett.* **78** 3133–5

[11] Baron T, Gentile P, Magnea N and Mur P 2001 *Appl. Phys. Lett.* **79** 1175–7

[12] Banerjee S, Salem M A and Oda S 2003 *Appl. Phys. Lett.* **83** 3788–90

[13] Porti M, Avidano M, Nafría M, Aymerich X, Carreras J and Garrido B 2005 *J. Appl. Phys.* **98** 056101

[14] Sze S M 1981 *Physics of Semiconductor Devices* 2nd edn (New York: Wiley)

[15] Huang S, Banerjee S, Tung R T and Oda S 2003 *J. Appl. Phys.* **93** 576–81

[16] Ioannou-Sougleridis V and Nassiopoulou A G 2003 *J. Appl. Phys.* **94** 4084–7

[17] Liu Y, Chen T P, Ding L, Zhang S, Fu Y Q and Fung S 2006 *J. Appl. Phys.* **100** 096111

[18] Busseret C, Souifi A, Baron T and Guillot G 2000 *Superlatt. Microstruct.* **28** 493–500

[19] Huang S, Banerjee S and Oda S 2002 *Mater. Res. Soc. Symp. Proc.* **686** A 8.8.1–8

[20] Ng T H, Chim W K, Choi W K, Ho V, Teo L W, Du A Y and Tung C H 2004 *Appl. Phys. Lett.* **84** 4385–7

[21] Lee J J and Kwong D L 2005 *IEEE Trans. Electron Devices* **52** 507–11

[22] Zhao D, Zhu Y and Liu J 2006 *Solid State Electron.* **50** 268–71