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Organic thin-film transistor memory with gold nanocrystals embedded in polyimide gate dielectric

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Abstract

An all-organic memory device based on a copper phthalocyanine (CuPc) thin-film transistor (TFT) using gold nanocrystals embedded in a polyimide gate dielectric is demonstrated. Both the gate dielectric and the active semiconductor layer are organic materials. Discrete gold nanocrystals are adopted as the charge storage medium. Under proper gate bias, gold nanocrystals are charged and discharged, resulting in the modulation of the channel conductance. Current–voltage (I–V) measurements at room temperature show the memory behaviour of the fabricated devices. The detailed programming and erasing operations are discussed. Low fabrication temperature and low cost are two benefits of the fabricated memory devices, which could provide a low-cost solution for the all organic circuits.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

In the past two decades, organic electronics have attracted considerable attention for their flexibility, low cost and large area process as a hot topic in both academia and industry. Many attractive applications such as radio-frequency identification tags [1], displays [2], organic solar cells [3] and large area sensors [4] have been proposed and demonstrated. Recently, much attention has been paid to organic memory devices. In this study, several types of memory devices based on organic and polymeric materials have been evaluated, including organic electrical bistable devices [5], organic–inorganic hybrid memory using a polymeric fuse [6] and a memory cell based on organic field-effect transistors (OFETs). Among all these types of organic memory devices, to make the memory cell based on an OFET is one potential option because of its non-destructive readout and single-transistor applications [7]. Up to now, two methods have been used to fabricate OFET memory devices. One way is to use a ferroelectric [8] or an electret which is a kind of chargeable dielectric [9]. In these cases, the direction of the polarization that occurs in ferroelectrics or the trapped charges in electrets modulates the channel conductance of transistors. Another way is to intentionally introduce charge traps, e.g. nanocrystals, into the gate dielectrics. This method has been widely exploited in the inorganic nanocrystal nonvolatile memory field [10,11], where complex fabrication and high-temperature process are typically involved, but hardly at all in the organic memory field. Recently, Kolliopoulou *et al* [12] reported a hybrid nanocrystal memory transistor with an organic control dielectric and an SiO_2 tunnelling oxide on the silicon channel. Liu *et al* [13] reported an OTFT stacked structure memory with a self-assembled gold nanoparticles embedded SiO_2 as a control oxide and poly(4-vinylphenol) (PVP) as a tunnelling layer. Leong *et al* [14] introduced a two-terminal capacitor structure organic memory by using pentacene as the active semiconductor layer, citrate-stabilized gold nanoparticles as the charge storage elements and SiO_2 as the insulator. All these works adopt an organic/inorganic hybrid structure and/or a silicon channel.

In this study, all-organic memory devices based on copper phthalocyanine (CuPc) thin-film transistors using a gold nanocrystals (nc-Au) embedded polyimide (PI) gate dielectric are fabricated and investigated. Both the gate dielectric and

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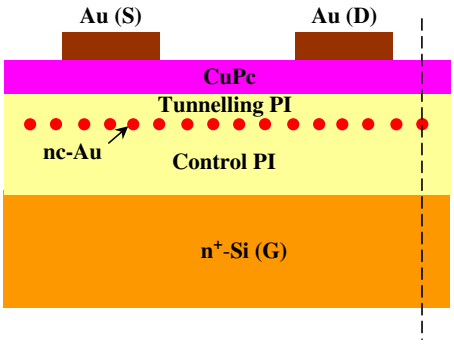

Figure 1. The schematic cross section of our organic nanocrystal memory with three sequential layers of PI/nc-Au/PI (with a thickness of 250/2/50 nm) as a whole insulator layer.

the active semiconductor layer are organic materials in this memory structure, which could provide a low-cost solution for the all organic circuits.

2. Experiment details

The device fabrication starts with cleaning of the heavily doped (1 0 0) n-type Si wafer (3.5×10^{-3} Ω cm), acting as the control gate electrode. The schematic cross section structure of the device is shown in figure 1. The stacked structure with three sequential layers of PI/Au/PI (with thicknesses of 250/2/50 nm) serves as the whole gate dielectric. The PI precursor is a polyamic acid which can be dissolved in n-methyl-2-pyrrolidinone (NMP). The polyamic acid solution is spin coated onto the substrate. The final thickness of the cured PI is controlled by varying the precursor/NMP solvent ratio and the spin speed. First, the control organic dielectric is formed through spin coating the polyamic acid solution (precursor/NMP = 2 : 1) at 4000 rpm, followed by soft baking at 100 °C for 20 min and then at 120 °C for 10 min to evaporate the solvent. Gold nanocrystals are obtained by e-beam evaporating a 2 nm thick Au wetting layer. The e-beam chamber pressure is 2.6×10^{-6} Torr. The deposition ramp for the thin Au wetting layer is 0.3 Å s^{-1} and the thickness of the Au layer is monitored by a quartz crystal oscillator. Then the Au/PI/n^+-Si structure is cured at 250 °C for 30 min. This step plays two main roles: one is to imidize the PI film and the other is to facilitate the formation of nc-Au. Later the surface morphology of some samples is characterized by a Hitachi S-4800 ultra-high resolution scanning electron microscope (SEM). The top PI layer is formed by spin coating the polyamic acid solution (precursor/NMP = 1 : 4) at 4000 rpm. The PI/Au/PI/n^+-Si structure is soft baked and fully cured again under the same condition. The final thicknesses of controlling and tunnelling gate dielectric layers are 400 nm and 50 nm, respectively. Later, a 50 nm thick organic semiconductor film CuPc as an active layer is deposited by thermal evaporation in vacuum. Finally, 50 nm thick gold top source/drain electrodes are evaporated and patterned by a shadow mask with a channel length of 40 μm and a width of 500 μm. Control samples without gold nanocrystals in polyimide dielectrics are simultaneously prepared with the same process for comparison. The

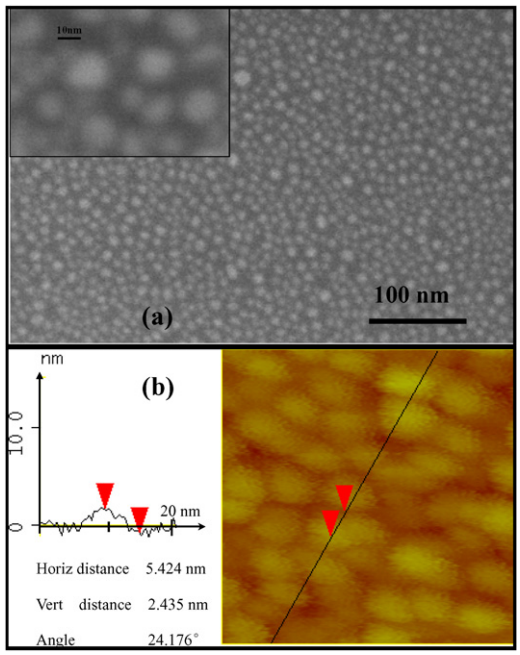

Figure 2. (*a*) The SEM image of gold nanocrystals on polyimide dielectrics and the local magnified image of surface morphology inserted. (*b*) The AFM image of nc-Au.

electrical characterization of the devices is performed with a Keithley 4200 semiconductor characterization system and a Cascade RF-1 probe station under ambient conditions.

3. Results and discussion

Figure 2(*a*) shows the SEM image and the local magnified surface morphology of gold nanocrystals on the polyimide dielectrics after a curing process of 250 °C for 30 min. And the AFM image of gold nanocrystals is also shown in figure 2(*b*). Discrete gold nanoparticles distribute well on the polyimide surface. As estimated, the mean surface nanocrystal density is about 5.6×10^{11} cm^{-2} and the average nanocrystal size is approximately 9–15 nm. It has been pointed out that an initial gold wetting layer with a thickness of around a few nanometres between two polyimide precursor layers can induce the formation of nanocrystals during the imidization of polyimide. The formation mechanisms of gold nanocrystals may be due to the weak interaction between gold and polyimide, which limits the wettability of Au on the PI surface during evaporation [15].

Figure 3 shows the output characteristic ($-I_{ds}$ and V_{ds}) of the transistor with the gate voltage (V_{gs}) from +20 to −20 V in steps of 10 V. It exhibits a good p-channel field effect transistor characteristic. Holes accumulate when negative V_{gs} is applied and deplete when positive V_{gs} is applied. A saturation of the drain current (I_{ds}) with increasing drain voltage (V_{ds}) is obtained even when zero V_{gs} is applied, a phenomenon known as the off-state drain leakage current [16].

The transfer characteristic ($-I_{ds}$ and V_{gs}) at $V_{ds} = -35$ V is shown in figure 4(*a*). The field-effect mobility μ of the fabricated device can be calculated using the equation [17]

$$I_{ds} = \frac{\mu W C_0}{2L}(V_{gs} - V_t)^2, \qquad (1)$$

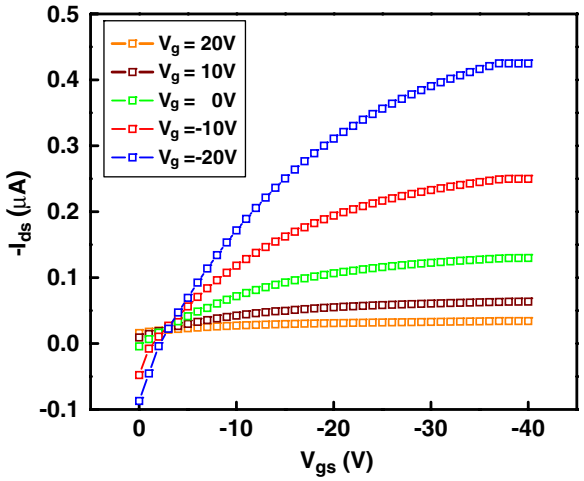

Figure 3. The output characteristic of gold nanocrystals CuPc-TFT with a channel length of $L = 40\,\mu$m, channel width of $W = 500\,\mu$m for different V_{gs}. All measurements are carried out at room temperature. The data shown here are taken in descending V_{gs} mode from +20 to −20 V in steps of 10 V.

where L is the channel length (40 μm), W is the channel width (500 μm) and C_0 is the capacitance per unit area of the gate insulator (10.8 nF cm^{-2} for our devices). C_0 is obtained from the Au/PI-nc-Au-PI/Au structure (not shown in here). The calculated value $\mu = 0.011\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ is consistent with other results reported for CuPc-based OTFTs [18]. It confirms that the presence of gold nanocrystals in the polyimide dielectric film does not affect the molecular structure and the arrangement of the CuPc thin film deposited.

An anticlockwise hysteresis loop is observed when a bi-direction scan voltage is applied to the gate electrode. The gate bias is swept from a positive voltage to a negative voltage and then returns to the initial value. Generally, hysteresis or the memory effect in OTFTs is due to the charge storage [9,13] and/or slow polarization [8] of the gate dielectric. To confirm the charge storage effect of gold nanocrystals embedded in the dielectric, a control sample without gold nanocrystals is tested. The transfer characteristic of the control sample is shown in figure 4(*b*). Negligible hysteresis is seen in the transfer characteristic of the control sample when the V_{gs} sweeps back and forth. Since the control sample has the same processing flow as the sample containing gold nanocrystals, the absence of hysteresis for the control sample can lead to the conclusion that the charging effect is attributed to the existence of gold nanocrystals.

The anticlockwise hysteresis direction indicates that when a negative gate bias is applied, holes are injected from the CuPc channel into the gold nanocrystals, corresponding to the programming process, and when a positive gate bias is applied, holes are ejected from the gold nanocrystals into the CuPc channel, corresponding to the erasing process. The gold nanocrystals as hole traps have been proved by Leong [14]. The injection or ejection of holes in the gate dielectric will lead to a threshold voltage (V_t) shift, which is the so-called memory window. As estimated from figure 4(*a*), a shift in V_t above 20 V is obtained after the gate bias sweeps back and forth.

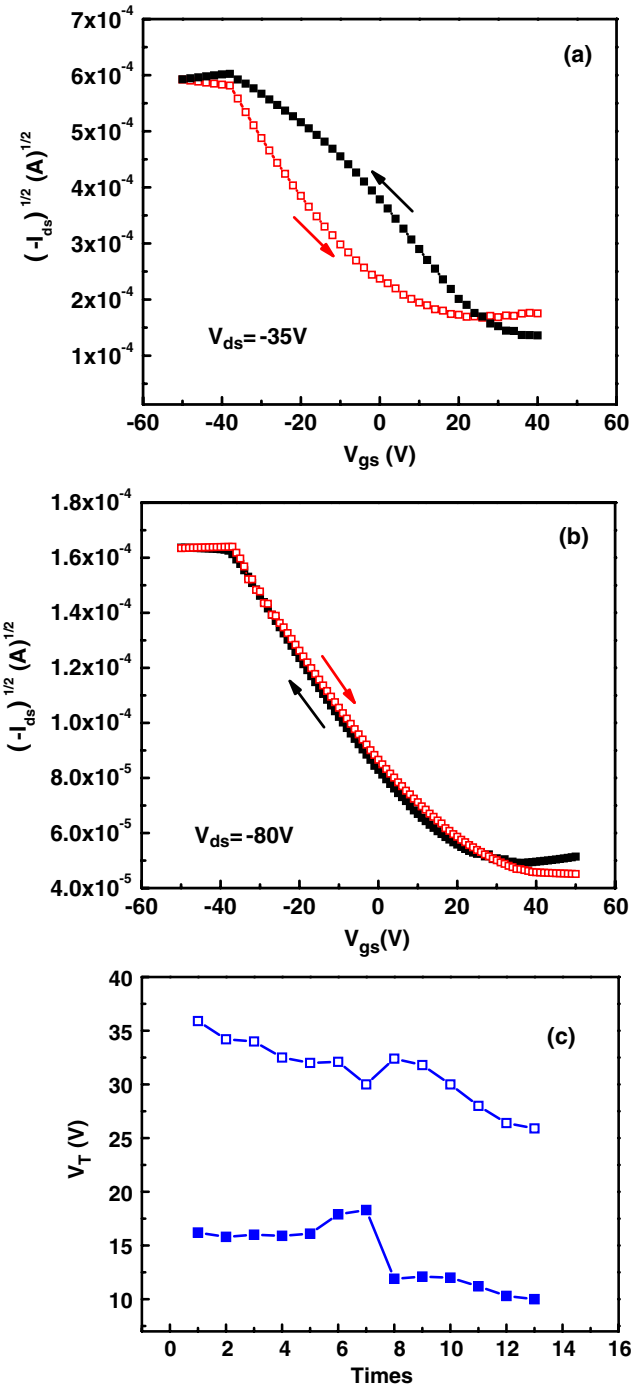

Figure 4. Transfer characteristics with bi-direction scan gate voltage (V_{gs}) ranges. The device with nc-Au embedded in polyimide gate dielectrics (*a*) and the control sample without nc-Au embedded (*b*). The V_{gs} bias is swept from a positive voltage (+50 V) to a negative voltage (−50 V) and returns to the initial value. In (*c*), the relationship between V_T for the different direction of the swept gate voltage and the tested times is shown. The open squares represent the V_T for the positive to the negative swept gate voltage and the solid squares represent the V_T for the negative to the positive swept gate voltage.

There are several mechanisms for charge exchange between nanocrystals and semiconductor channels for Si-based metal nanocrystal memory devices. The hot-carrier injection mechanism, the direct tunnelling mechanism and the Fowler–Nordheim (FN) tunnelling mechanism are the three

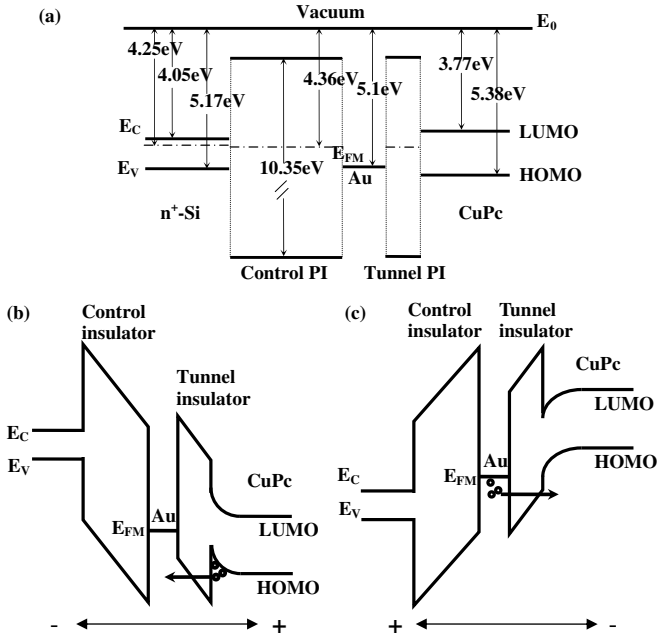

Figure 5. The energy level diagram of CuPc/PI/nc-Au/PI/n$^+$-Si (along the dashed line shown in figure 1) (*a*) and the schematic energy-band variation diagrams during the program (*b*) and the erase (*c*) operations of the p-channel organic transistor memory device.

main programming/erasing (P/E) mechanisms [11]. In organic memory devices, however, things are different. Due to the low carrier mobility (0.011 cm^2 V^{-1} s^{-1} in our case) of the organic semiconductor, the drift velocity ($v = \mu$E) in an OTFT should be several orders of magnitude smaller than that in a silicon based transistor, under the same electric field E. And for direct tunnelling, an ultrathin tunnelling dielectric layer is used to separate the nanocrystals from the channel. Here a polyimide tunnelling layer of around 50 nm is used. Thus, hot-carrier injection and direct tunnelling could be excluded and the FN tunnelling should dominate the transfer mechanism for the organic memory devices.

Figure 5(*a*) shows the energy level diagrams of CuPc/PI/nc-Au/PI/n$^+$-Si (along the dashed line shown in figure 1), where E_C and E_V are the energy level of the conduction band edge and the valence band edge of Si (4.05 eV and 5.17 eV, respectively) [19]. E_0 is the vacuum energy level. E_{FM} is the work function of Au (5.1 eV) [19]. LUMO and the HOMO are the lowest unoccupied molecular orbital and the highest occupied molecular orbital of CuPc (3.77 eV and 5.38 eV, respectively) [20]. The work function and the energy-band gap of polyimide dielectric are 4.36 and 10.35 eV [21]. The schematic energy-band structure variations corresponding to P/E processes are shown in figures 5(*b*) and (*c*). The quantity of this energy level variation is quite complex. Here, a qualitative explanation is given to illustrate the P/E processes. When a large negative voltage is applied to the gate electrode for a while, LUMO and HOMO of CuPc and polyimide bend upwards very much, so that the holes in the channel have chances of being transferred from the channel to the gold nanocrystals floating gate through the FN tunnelling process and of being captured in the gold nanocrystals as shown in figure 5(*b*), then the programming is performed. The captured holes generate an internal electric field along the direction opposite to the applied negative voltage and this internal electric field weakens the external applied electric field effects. A more negative gate voltage is needed to turn the device on; that is, a left shift of the threshold voltage occurs. As shown in figure 4(*a*), when the gate voltage sweeps from the negative value, the I–V curve (open squares) of the OTFT shifts to the left. Similarly, when a relatively large positive voltage is applied to the gate electrode for a moment, the orbital energy level bends downwards and the holes stored in the gold nanocrystals are ejected back into the CuPc channel through FN tunnelling, as shown in figure 5(*c*), and then the erasing process is performed. Since the internal electric field induced by the captured holes disappears which prevent the device from turning on, a smaller gate voltage is needed to turn it on. A right shift of the threshold voltage occurs. As shown in figure 4(*a*), when the gate voltage sweeps from the positive value, the I–V curve (solid squares) relatively shifts to the right. Thus a P/E cycle is done. We do the operation like this for several times to confirm its repeatability. The relationship between the threshold voltage and the tested times is shown in figure 4(*c*). The open squares represent the V_T for the positive to the negative swept gate voltage and the solid squares represent the V_T for the negative to the positive swept gate voltage. As seen, ΔV_T is around 20 V for every gate voltage sweeping back and forth.

4. Conclusions

In summary, an all-organic memory device based on a CuPc thin-film transistor using gold nanocrystals embedded in a polyimide gate dielectric has been fabricated and electrically characterized. Both the gate dielectric and the active semiconductor layer are organic materials. Discrete gold nanocrystals are adopted as the charge storage medium. Current–voltage (I–V) measurements at room temperature show the memory behaviour of the fabricated devices. Possible operating mechanisms corresponding to the programming and the erasing processes are discussed on the basis of the I–V curves and energy-band structures. Under a proper gate bias, gold nanocrystals are charged and discharged, resulting in the modulation of the channel conductance. Low fabrication temperature and low cost are two benefits of the fabricated memory devices, which could provide a low-cost solution for the all organic circuits.

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