IOP PUBLISHING JOURNAL OF PHYSICS D: APPLIED PHYSICS

J. Phys. D: Appl. Phys. **41** (2008) 035109 (5pp) doi:10.1088/0022-3727/41/3/035109

Comparison of discrete-storage nonvolatile memories: advantage of hybrid method for fabrication of Au nanocrystal nonvolatile memory

Qin Wang[1], Rui Jia[1], Weihua Guan[1], Weilong Li[1], Qi Liu[1], Yuan Hu[1], Shibing Long[1], Baoqin Chen[1], Ming Liu[1,3], Tianchun Ye[1], Wensheng Lu[2] and Long Jiang[2]

[1] Key Laboratory of Nano-fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China
[2] Key Laboratory of Colloid and Interface Science, Centre of Molecule Sciences, Institute of Chemistry, Chinese Academy of Sciences, Beijing 100029, People's Republic of China

E-mail: liuming@ime.ac.cn

Received 12 July 2007, in final form 19 December 2007
Published 11 January 2008
Online at stacks.iop.org/JPhysD/41/035109

Abstract

In this paper, the memory characteristics of two kinds of metal-oxide-semiconductor (MOS) capacitors embedded with Au nanocrytals are investigated: hybrid MOS with nanocrystals (NCs) fabricated by chemical syntheses and rapid thermal annealing (RTA) MOS with NCs fabricated by RTA. For both kinds of devices, the capacitance versus voltage (C–V) curves clearly indicate the charge storage in the NCs. The hybrid MOS, however, shows a larger memory window, as compared with RTA MOS. The retention characteristics of the two MOS devices are also investigated. The capacitance versus time (C–t) measurement shows that the hybrid MOS capacitor embedded with Au nanocrystals has a longer retention time. The mechanism of longer retention time for hybrid MOS capacitor is qualitatively discussed.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Since the introduction of silicon nanocrystals (NCs) as a replacement for the conventional floating gate in the nonvolatile memory (NVM) structure by Tiwari *et al* [1], NC memories are considered as one of the promising candidates for future nonvolatile, high density and low-voltage memory applications, owing to their inherent immunity to the local oxide defect by discrete charge storage, which allows more aggressive scaling of the tunnelling oxide thickness. Among the efforts for further improving the performance of NC memories, metal NC was proposed as against its semiconductor counterpart due to large density of states, three-dimensional electric field enhancement and selectable work function. It has been shown that the larger work function of the metal NC than that of the silicon NC is the key to reducing the leakage current through the tunnelling barrier owing to the increased electron barrier, which is nicknamed as work-function engineering [2, 3]. However, the traditional technique for the growth of metal NCs involves conventional deposition processes such as electron beam evaporation, sputtering and chemical vapour deposition, followed by rapid thermal annealing (RTA) at temperatures close to its eutectic point. The high temperature gives the atoms enough surface mobility to self-assemble into NCs which also recedes the character of NVM. At the same time diffusion of metal atoms into the oxide layer also occurs. As a result, the leakage current is large and the retention time is short. To block the diffusion of metal atoms and then increase the retention time, some of the processing techniques such as NH_3 ambient was introduced during the annealing, as published elsewhere [4]. But in this

[3] Author to whom any correspondence should be addressed.

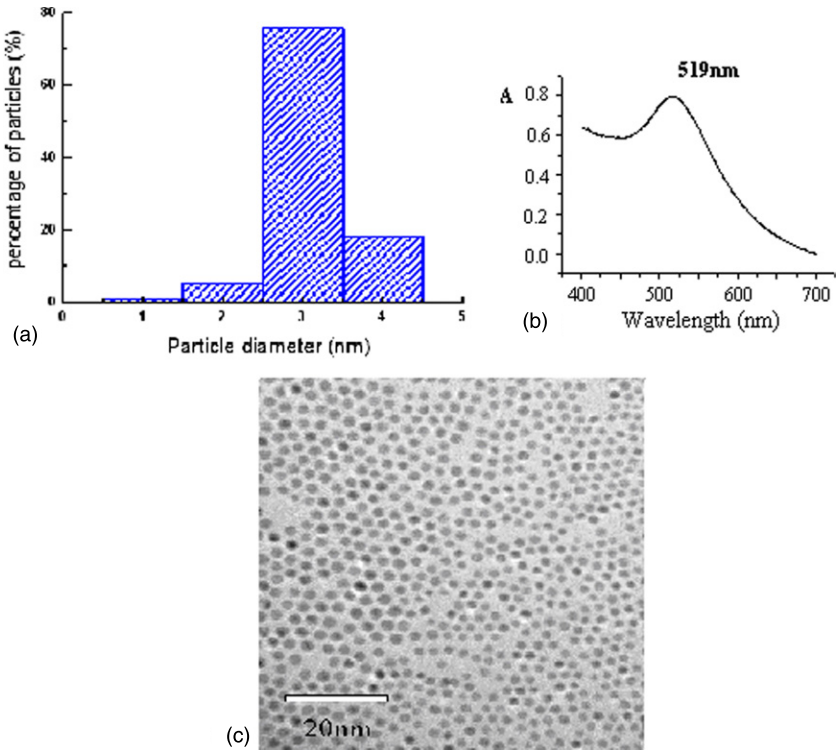

Figure 1. (*a*) The histogram of the Au NCs' size distribution formed by the hybrid method, (*b*) the UV-visible absorption spectrum of Au NCs and (*c*) the TEM graphics.

study, we try to fabricate hybrid metal-oxide-semiconductor (MOS) capacitors embedded with chemically synthesized Au NCs to avoid the thermal processing, which is more favourable for fabricating the NVM device with a larger memory window and a longer retention time, as opposed to the MOS NVM devices embedded with Au NCs formed by RTA.

2. Experimental

2.1. Chemical syntheses of Au NCs

The syntheses of Au NCs were similar to that described by Lin *et al* [5]. In this research, $HAuCl_4$, $4H_2O$, hexane, toluene, sodium dorohydride, 1-dodecanethiol and distearyldim-thyl-ammonium bromide (DTAB) were used to synthesize Au NCs. All reagents were of analytical grade. First of all, 6 ml aqueous solution of $HAuCl_4$ (1%) in a 250 ml cone-shaped bottle was vaporized to remove water. Then 80 ml toluene and 0.18 g of DTAB were added to the bottle. Both $HAuCl_4$ and DTAB were dissolved in toluene by sonication. Subsequently, 0.3 ml of $NaBH_4$ (0.056 g in water) was added to the solution under vigorous stirring and a red-coloured gold colloid was synthesized in several minutes. After 1 h, 0.8 ml of 1-dodecanethiol was added dropwise to the colloid to modify the gold surface through a ligand exchange reaction. Afterwards, the gold nanoparticles with 1-dodecanethiol as protective molecules were concentrated to about 3 ml under vacuum conditions and precipitated with ethanol and then separated by centrifugal sedimentation. The precipitation, which was re-dispersed with 10 ml toluene and 0.8 ml 1-dodecanethiol in a flask, was refluxed for 3 h. After being refluxed, the mixture was placed at room temperature (RT) overnight in the flask. The supernatant solution was separated for the next experiment with centrifugal sedimentation, and ethanol was added to the supernatant solution to precipitate monodisperse gold nanoparticles. Figure 1 shows the histogram of size distribution, the UV-visible absorption spectrum of as-prepared gold nanoparticles and the TEM graphics, respectively. The size of spherical gold nanoparticles is mainly distributed in the range 2.5–3.5 nm. The average diameter is determined to be 3.0 nm from this histogram with a standard deviation of 0.22. By this means, the synthesized gold NCs are monodispersed and uniformly dispersed in the solvent; they are stable and will not conglomerate. The colloidal Au NCs solution can be kept for a long time. This is because the protective molecules adsorbed by the Au NCs, which were formed during the syntheses and denoted by the $C_{12}H_{25}SH$ molecule, cause the repulsion force between particles, as shown in figure 2.

3. Device fabrication of NC NVM with MOS structure

In this research, two kinds of MOS capacitors with NCs embedded in the gate oxide were fabricated: hybrid MOS NVM and RTA MOS NVM. Figure 3 shows the schematic cross-sectional structure of the MOS capacitor discussed in this paper. Firstly, (1 0 0)p-type silicon wafers underwent the standard H_2SO_4/H_2O_2 and the diluted HF solution cleaning processes and then a 5 nm SiO_2 tunnelling layer was thermally grown onto the Si (1 0 0) in dry oxygen ambient at 900 °C, denoted by SiO_2 (5 nm)/Si . Here 5 nm was the data from

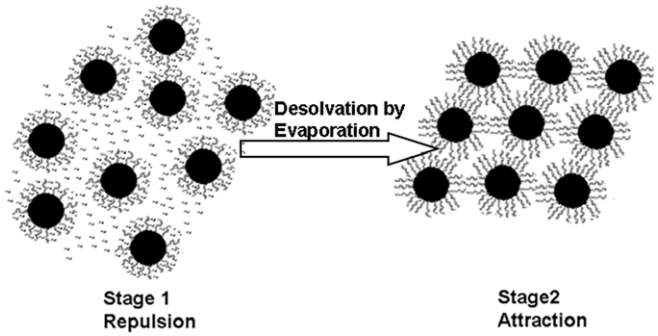

Figure 2. Schematic illustration of the interaction between nanoparticles over the period of evaporation. On the left side is the picture at the beginning stage of the 2D arrangement; the right side presents the closed packing of nanoparticles after solvent evaporation, where the ligand molecules on particles are ordered.

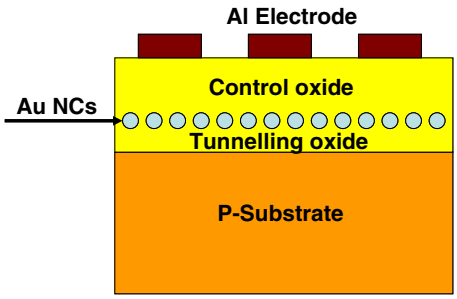

Figure 3. Schematic cross-sectional structure of the fabricated capacitor structure.

technician's experience, and the thickness in practice should be less than that.

For the hybrid MOS NVM, the aforementioned colloidal Au NC precursor was spinning-coating onto the SiO_2(5 nm)/Si wafer at 3000 r min^{-1} for 40 s to evaporate the solvent. The wafer was then uniformly capped by Au NCs. Although the spinning rate can be changed significantly, the surface density of Au NCs, according to our experiment results, does not change so much. In contrast, the surface density of Au NCs is mainly determined by the volume density of Au NCs in the precursor. Hence, the changing volume density can adjust the surface density of Au NCs. As to the fabrication of RTA MOS NVM, firstly, a thin Au wetting layer was deposited onto the SiO_2(5 nm)/Si wafer through the e-beam evaporation with the deposition ramp of 0.5 Å S^{-1} and the chamber pressure of 3×10^{-6} Torr. The thickness of the thin metal layer was precisely monitored by a quartz crystal oscillator. After the deposition of the 2 nm Au film, RTA was carried out in N_2 ambient at 600 °C for 30 s to transfer the Au film into NCs. During the fabrication, the NCs were characterized by a HITACHI S-4800 ultra-high resolution scanning electron microscope (SEM). Then, both the hybrid MOS NVM and the RTA MOS NVM were put into a plasma enhanced chemical vapour deposition (PECVD) chamber and a thin layer of 25 nm SiO_2 was simultaneously deposited as the control oxide with the furnace temperature at 280 °C. After this step, 200 nm Al top electrodes with an area of 10^{-3} cm^2 were deposited by e-beam evaporation. At the same time, the reference sample without any Au NCs was fabricated with the same processes. The charge storage characteristics of Au NCs in SiO_2 were analysed by high-frequency (1 MHz) capacitance–voltage (C–V) with a Keithley 4200 precise semiconductor analyzer and a Keithley 590 C–V analyzer at RT. And the START TIME and the STEP TIME were manually set to 1 s and 0.1 s, respectively. The charge retention behaviours were also characterized by the transient capacitance (C–t) measurement techniques.

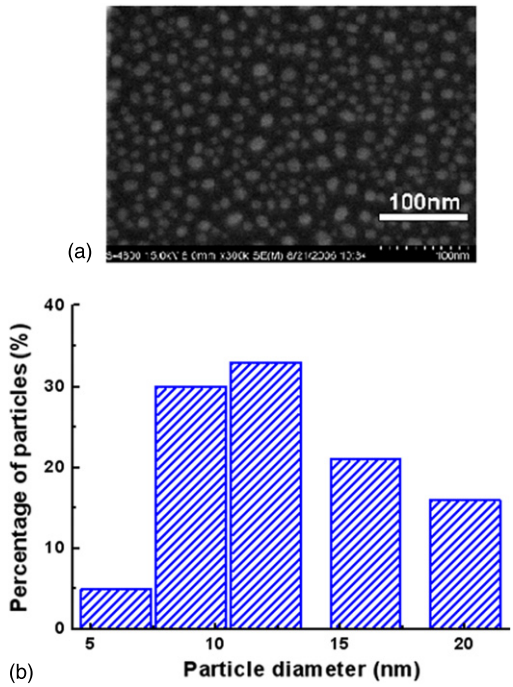

Figure 4. (*a*) The SEM of Au NCs formed by the RTA process and (*b*) the histogram of NCs' size distribution.

4. Result and discussion

Figure 4(*a*) shows the SEM micrograph of the Au NCs formed by RTA, and figure 4(*b*) shows the NCs' size distribution for the Au NCs. It can be seen that the NCs' shape is nearly round, but the size distribution is large—varying from 5 to 20 nm. Since the formation of NCs is achieved through the relaxation of film stress and limited by the surface mobility, some long range forces such as the dispersion force and the electrical double layers will also affect the NC size and the location distributions [6, 7]. Here, it is worth noting that the NC density and the size distribution can be controlled by the initial film thickness, which was already proved by our results and other groups' research [8, 9]. Because this self-assembly is a thermodynamic process in nature, the annealing temperature and profile will also affect the NCs' geometry. The NC density and size distribution can be controlled to some extent through the initial film thickness and annealing profile in a similar fashion. Hence, we choose a 2 nm Au film to be the as-deposited film since it forms NCs with a minimum size at 600 °C, with a typical NC density of 3×10^{11} cm^{-2} and a NC size in the 5–20 nm range, as opposed to 2.5–3.5 nm of NCs synthesized by the chemical way. Hence, the size of chemically synthesized Au NCs is smaller and more uniform than those of NCs formed by RTA.

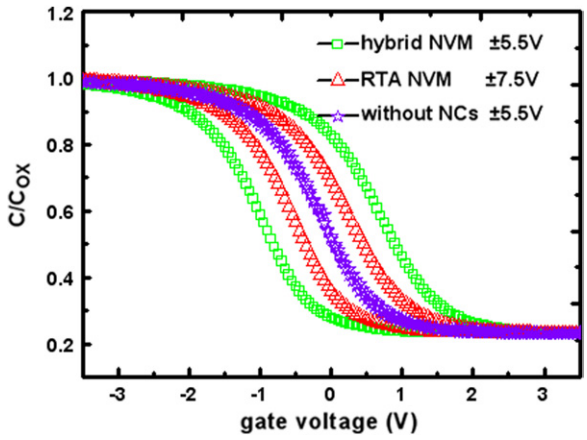

Figure 5. C–V characteristics for both hybrid MOS NVM and RTA MOS NVM.

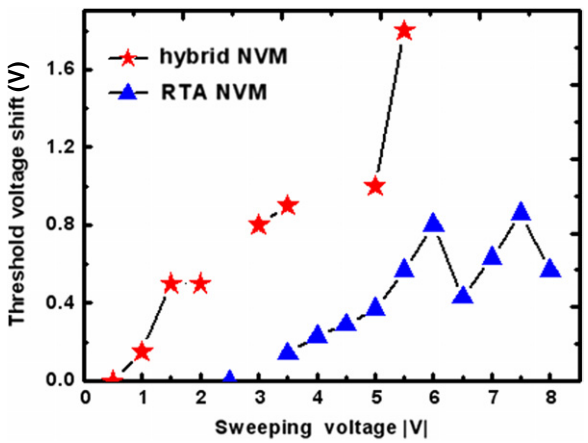

Figure 6. The comparison of the memory windows versus the P/E voltage for RTA MOS NVM and hybrid MOS NVM.

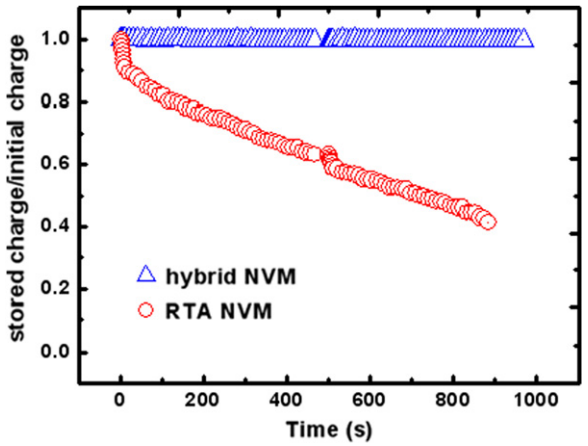

Figure 7. C–t measurement for both samples.

It is known that the as-deposited film is got naturally with some thickness perturbation. When it is RTA treated to give the atoms enough surface mobility, the film will be relaxed into a lower total-energy state. To reduce the elastic energy carried by the stress built into the film during the deposition process, the film tends to break into islands along the initial perturbation. However, minimization of the surface energy and the dispersion force between the top and bottom interfaces can help stabilize the film. So the final geometry will depend on the balance of these driving forces. Once the NCs are formed, the work-function difference between the metal and the extrinsic substrate generates a localized depletion or accumulation region in the substrate. The repulsion force between those regions helps stabilize the NCs and keep a uniform spacing.

The charging characteristics for both hybrid MOS NVM and RTA MOS NVM were analysed by the 1 MHz C–V measurement, as shown in figure 5. In order to do the comparison, the ordinary MOS device without the embedded NCs was also characterized and plotted in figure 5. The dc gate bias was swept from a negative voltage to a positive voltage and then returned back to the initial value, which corresponded to the accumulation and inversion behaviours.

As shown in figure 5, the C–V curve of the ordinary MOS device without NCs exhibits negligible hysteresis. For both hybrid MOS NVM and RTA MOS NVM, however, remarkable counterclockwise hysteresis was observed when the gate bias was swept back and forth. The observed counterclockwise hysteresis is attributed to the charging and discharging process in the MOS capacitor structure. When a positive bias is applied, electrons are injected from the inversion layer of the Si substrate to the gate oxide matrix. When a negative bias is applied, electrons are ejected from the MOS gate matrix to the Si substrate. Hence, the electron charging is the dominant mechanism in both the hybrid MOS NVM and the RTA MOS NVM. The injection or ejection of electrons leads to flat band voltage shift, the so-called memory window. It can be clearly seen that when the gate sweeping voltage is the same, the V_{FB} shift of hybrid MOS NVM is larger than that of RTA MOS NVM, and the magnitude of the memory window is found to be dependent on the voltage sweeping range. In order to see the sweeping voltage dependences of the memory window for these two devices, the sweeping voltage versus V_{FB} curves were plotted in figure 6. Surprisingly, it is found that when the programming/erasing (P/E) voltage is the same, the hybrid MOS NVM shows a larger flat band voltage, as compared with RTA MOS NVM. That is to say, the former has better charging characteristics than the latter. Anyway, the memory window is found to increase with increasing gate bias, indicating more charges are injected. Generally, the number of charge carriers stored in the NCs can be estimated by the relation $Q = C V_{FB}$, where C is the capacitance density and V_{FB} is the flat band voltage shift. From this relation, when the sweep voltage is in the range of ± 5.5 V, the number of charge carriers stored in the Au NCs is about 2×10^{11} cm^{-2}.

In order to investigate the charge storage and retention characteristics of both kinds of devices, C–t measurements are performed at RT, as shown in figure 7. It can be seen that the charge loss rate by the film deposition of Au NCs is greater than that with the hybrid Au NCs. The hybrid MOS NVM has a longer retention time and less charge loss. Here, it is necessary to analyse the charge loss path. As we can see from figure 8, for electrons, there are three main discharging paths: 1—discharging from NCs to the control

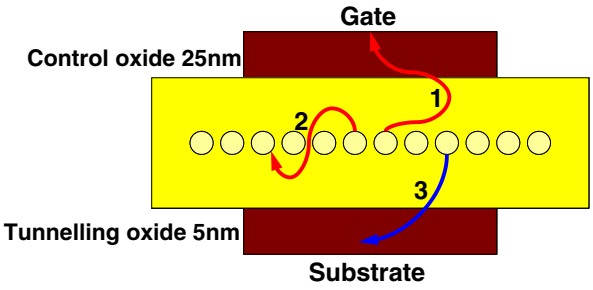

Figure 8. The potential discharging paths for MOS devices embedded with Au NCs.

gate, 2—discharging from one NC to the adjacent NCs, and 3—discharging from the NCs to the substrate. Since the 25 nm thick control dielectric is five times thicker than the tunnelling dielectric, discharging current via the control dielectric can be neglected. The discharging current from one NC to the adjacent NCs can be neglected. This is reasonable due to the strong Coulomb block effect of the NC and the large spacing between NCs. In our devices, the discharging current during retention is dominated by electrons tunnelling out from NCs to the substrate. Since the control gate is zero biased during retention and the number of charges stored in the NCs is limited, the electric field in the tunnelling dielectric is low. The tunnelling mechanism, therefore, for both kinds of devices is direct tunnelling. Here it should be worth noting that all kinds of devices have the same fabrication process except that the RTA MOS NVM undergoes the RTA process. Hence, the charge loss for the RTA MOS NVM is larger than the hybrid MOS NVM from NCs to the substrate via the tunnelling oxide layer. Here, it is reasonable to believe that by the RTA process, high temperature annealing not only provides the atoms with sufficient surface energy to form the NCs but also enables them to diffuse into the thin dielectric tunnelling oxide. The metal atoms' diffusion degrades the insulation of the tunnelling oxide and can form leakage paths from NCs to the substrate, which is also proved by Tan *et al* [4]. Thus, it naturally causes the degradation of the retention characteristics. However, for the hybrid MOS NVM embedded with Au NCs, all the processes are performed at RT, and there is not enough energy for the metal atoms to diffuse into the tunnelling oxide. It thus results in the improvement of the retention characteristics.

5. Conclusions

In conclusion, we have demonstrated the realization of a hybrid memory device, in which chemically synthesized Au NCs are dispersed by spin coating on the oxide p-type Si substrate embedded between the tunnelling oxide and the control oxide. It is found that the hybrid memory device has a longer retention time and a larger memory window, as opposed to the RTA MOS memory device with Au NCs formed by high temperature RTA processes. This is due to no thermal processing for hybrid memory devices, as opposed to the RTA MOS memory device, for which the high temperature RTA process helps to diffuse Au atoms into the tunnelling oxide and causes the discharging paths from the NCs to the substrate. This result offers us a good opportunity to significantly improve the memory device performance based on the hybrid process.

Acknowledgment

This work was partly supported by the National Basic Research Program of China (973 Program) under Grant No 2006CB302706 and the National Natural Science Foundation of China under Grant Nos 90607022, 90401002, 60506005, 60390071, 60706023, CAS YZ0635 and Bai Ren Ji Hua support.

References

[1] Tiwari S, Rana F, Hanafi H, Hartsten A, Crabbe E F and Chan K 1996 *Appl. Phys. Lett.* **68** 1377–9
[2] Liu Z, Lee C, Narayanan V, Pei G and Kan E C 2002 *IEEE Trans. Electron Devices* **49** 1606–13
[3] Liu Z, Lee Z, Narayanan V, Pei G and Kan E C 2002 *IEEE Trans. Electron Devices* **49** 1614–21
[4] Tan Z, Samanta S K, Yoo W J and Lee S 2005 *Appl. Phys. Lett.* **86** 013107
[5] Lin X M, Jaeger H M, Sorensen C M and Klabunde K J 2001 *J. Phys. Chem.* B **105** 3353
[6] Suo Z and Zhang Z 1998 *Phys. Rev.* B **58** 5116
[7] Bonnell D A, Liang Y, Wagner M, Carroll D and Bühle M 1998 *Acta Mater.* **46** 2263
[8] Guan W H, Long S B, Liu M, Li Z G, Hu Y and Liu Q 2007 *J. Phys. D: Appl. Phys.* **40** 2754
[9] Guan W H, Long S B, Liu M, Li Z G, Hu Y, Liu Q and Jia R 2007 *Solid State Electron.* **51** 806–11