A Coordinating Control for Hybrid HVDC Systems in Weak Grid

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***Abstract*—A coordinating control strategy is proposed for a Hybrid High Voltage DC (HVDC) system comprising a Capacitor Commutated Converter (CCC) connected in series with a 2-stage Voltage Source Converter (VSC) called 'Vernier'. This approach ensures (a) the tap changers and switched capacitor banks are eliminated by Vernier controls that maintain constant firing angle and margin angle at the rectifier and inverter, respectively, and provide volt-VAr control at the commutation bus (b) improves the power flow recovery and risk of commutation failure following sever faults. To that end, a detailed switched model of Hybrid-HVDC is built in EMTDC/PSCAD platform. For frequency-domain analysis, a new nonlinear state-space averaged model is also developed and benchmarked against the detailed model. The steady-state operating characteristics of the proposed Hybrid HVDC system is established. Finally, the effectiveness of the proposed approach is demonstrated for weak AC systems interfacing the rectifier and inverter sides. Improvement in commutation failure and power flow recovery following severe disturbances are also shown through case studies.**

***Index Terms*—CCC, Hybrid HVDC, VSC, weak grid.**

I. Introduction

Hybrid High Voltage DC (HVDC) concepts have been proposed by researchers in multiple forms, which involve Line Commutated Converters (LCCs) and Self Commutated Converters (SCCs), e.g. Voltage Source Converters (VSCs). The motivation behind such Hybrid schemes is primarily driven by their ability to work in weak AC grids, or in the worst case serving isolated loads. One architecture considers an LCC station in one end of the HVDC transmission system and an SCC station at the other end - examples include [1]–[11]. In [12], a three-terminal HVDC system with two LCC and one SCC stations was proposed.

Another architecture [13]–[15] considers LCC at the rectifier-end and a Hybrid topology at the inverter-end. The Hybrid topology in [13]–[15] consists of LCC and VSC connected in series in the DC side and in parallel in the AC side. In these papers, the main objective of bringing in VSC in the inverter-end is to provide voltage regulation functionality in the commutating bus interfaced with a weak AC grid. The VSC maintains a constant DC voltage in its DC-bus. As a result there is no independent control of real power flow through the VSC. In effect, control coordination among the LCC and the VSC converters is absent in this scheme. The rating of the VSC was 30% of the LCC rating, which was designed to minimize the cost.

TABLE I
Existing literature on types of point-to-point Hybrid system

Category	References	Comment
LCC on one side & VSC on other	[1]–[11]	One of the sides is considered strong. The scenario where the grids are weak on both the ends has not been considered. Severe fault cases have not been investigated.
LCC on rectifier & Hybrid on inverter	[13]–[15]	Inverter-side LCC and VSC are in series on DC side and in parallel on AC side. VSC maintains a constant DC voltage in its DC-bus, thus no independent control of real power flow through the VSC.

In contrast to the literature mentioned above (summarized in Table I), this paper presents a coordinating control for Hybrid HVDC converter systems, which was first proposed by Chaudhuri et-al in [16]. *Reference [16] is a patent literature, which did not report any analytical modeling, insightful frequency-domain analysis, steady-state operating characteristics, and dynamic performance of the proposed topology.* Hybrid-HVDC converter system presented in this paper consists a Capacitor Commutated Converter (CCC) [17]–[20] coupled in series with a 2-stage VSC, called '*Vernier*,' on DC side [16] - see Fig.1. For a 500kV DC transmission voltage, the Vernier consists of 2-level AC-DC stage and a DC-DC stage with DC voltage of $\pm 40kV$. The 2-level VSC installations considering voltage ranging from $9kV$ to $150kV$ have been reported in literature [21], [22]. Thus, it is possible to reach $40kV$ voltage rating of the Vernier with a 2-level structure. With the advancement of IGBT, the rating of the device has improved from $2.5kV$ to $6.5kV$ (SPT - IGBT HiPak module) in terms of voltage [23] and IST^{+} IGBT HiPak2 module [24] offers $3600A/1700V$ current/voltage rating. Considering the practical feasibility of the topology presented, the main contributions of the paper are:

(1) A coordinating control strategy is proposed, which ensures that - (a) CCC and Vernier equitably share the control burden, (b) the tap changers and switched capacitor banks are eliminated by Vernier controls that maintain constant firing angle and margin angle at the rectifier and inverter, respectively, and (c) Vernier provides volt-VAr control at the commutation bus.
(2) A new nonlinear state-space averaged model for the proposed system has been developed for the frequency-domain

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analysis of progressively weak AC grid. This model is benchmarked against a detailed switched model.
(3) The operating characteristics of the proposed Hybrid HVDC system is established.
(4) The effectiveness of the proposed approach in terms of recovery of power flow and commutation failure following severe disturbances is demonstrated through time-domain simulation for weak AC systems.

It should be noted that the proposed Hybrid topology can result in savings in real-estate and reduce cost by eliminating tap changing transformers and switched capacitors. However, this comes at an expense of the Vernier with nearly 10% rating of CCC. We don't claim that the Hybrid solution is cheaper and emphasize that a cost analysis is outside the scope of this paper. On the contrary, the focus is on proposing a coordinating control, which is missing from Hybrid HVDC-related papers in the literature [1]–[15].

II. LCC HVDC System

Typical LCC HVDC systems as shown in Fig. 2 need a large switchyard with capacitor banks and filters at each converter-end.

The capacitor banks are switched in or out with larger change in loading condition to match the reactive power demand of the converters. Following a change in loading conditions and grid-side disturbances, the tap changing transformers (Fig. 2), act to slowly regulate the converter-side AC voltages to bring the rectifier-side firing angle α_r and inverter-side margin angle γ_i to the pre-disturbance-level. In addition to tap changing transformers, whose life reduce with frequent operations; a significant real estate and cost is incurred by the switchyard. Moreover, weak AC grids cause serious issues in operating LCC HVDC systems. To solve the above issues, we present a Hybrid HVDC system and a coordinating control, first proposed by Chaudhuri et-al [16].

III. Hybrid HVDC System

A. Architecture & Overall Goals

The Hybrid-HVDC converter system presented in this paper includes a CCC coupled in series with a 2-stage VSC, called '*Vernier*', on DC side [16] - see Fig. 1. The Vernier consists of a number of smaller units connected in series in the DC-side and in parallel in the AC-side. Each vernier unit consists of an AC-DC stage and a DC-DC stage shown in Fig. 4. The combination of CCC and Vernier with DC voltages V_{CCC} and V_{ver}, respectively, regulates the net DC voltage V_{dc} at the converter station DC terminals. As shown in Fig. 1, this scheme aims to achieve the following:

- significantly reducing the switched capacitors by maintaining net reactive power consumption almost constant over a range of operating conditions,
- eliminating the use of converter-transformer tap changers both at rectifier and inverter bus by DC voltage regulation through Vernier,
- enhancing power flow recovery and reducing commutation failure following severe disturbances.

B. Desired Steady State Performance

The idea of the proposed Hybrid scheme is inspired by measuring length in coarse terms using a meter scale in conjunction with obtaining a finer resolution using a Vernier scale. Functionally, 'Vernier' will be responsible to alter its DC voltage V_{ver} to follow the commanded DC current flow (or reference converter DC voltage) while ensuring that the converter firing angle (or margin angle) is maintained at its lowest value α_{min} (or γ_{min}), thereby consuming the smallest amount of reactive power. This will require the Vernier voltage to be adequate enough to account for the voltage drop in the DC line with change in loading conditions. With change in E_{acr} and E_{aci}, V_{ver} should also change to ensure operation of the CCC at α_{min} or γ_{min}. This will help the AC-DC converter of the Vernier (Fig. 4) to operate with unity power factor, thereby reducing the converter rating.

When the operation is outside expected nominal range, V_{ver} might hit its limit and the converter firing angle α (or margin angle γ) will increase beyond its minimum value.

C. Desired Dynamic Performance

Under dynamic condition, e.g. following system disturbances or change in controller references, both firing angle α and V_{ver} will change. The goal is to employ a coordinating control that is expected to:

- seamlessly share the control burden among the CCC and the Vernier during dynamic condition
- ensure that the Vernier voltage limit hitting is avoided as much as possible
- perform smoothly without any controller switching when the Vernier moves in and out of saturation
- provide volt-VAr control at the commutation bus when AC voltage is within a pre-defined range and perform voltage regulation beyond that using the AC-DC converter of the Vernier (Fig. 4).

The proposed coordinating control strategy is described next.

IV. Proposed Coordinating Control Strategy

A. Rectifier-side Control

The proposed coordinating control strategy for the rectifier is shown in Fig. 3. In normal condition, the rectifier operates under current control (CC) mode, which produces a voltage command V^*_{dcr} corresponding to the total DC voltage at the rectifier-end. As shown in Fig. 3, this command is split between the CCC and the Vernier:

$$\begin{aligned} V^*_{dcr} &= K_{pr}\left(I^*_{dr} - I_{dr}\right) + K_{ir}\int\left(I^*_{dr} - I_{dr}\right)dt \\ V^*_{dcr} &= V^*_{CCCR} + V^*_{verR} \end{aligned} \tag{1}$$

The Vernier voltage reference is synthesized using the following relationship:

$$\begin{aligned} V^*_{verR} &= K_{verR}\int dV^*_{dcr} + K_{\alpha r}\int\left(\alpha^*_{r\_\min} - \alpha^*_r\right)dt \\ &+ \int \Delta_{bleedr}dt \end{aligned} \tag{2}$$

where, Δ_{bleedr} is the output of a bleeder scheme, which is -ve (+ve) if the DC-link voltage V_{dcverR} of the Vernier, shown in Fig. 1, falls below (goes above) a threshold.

Figure 5 shows the Vernier's AC-DC converter control. The AC-DC converter (Fig. 4) is responsible for maintaining the DC-link voltage V_{dcverR} through controller gains K_{pDC} and

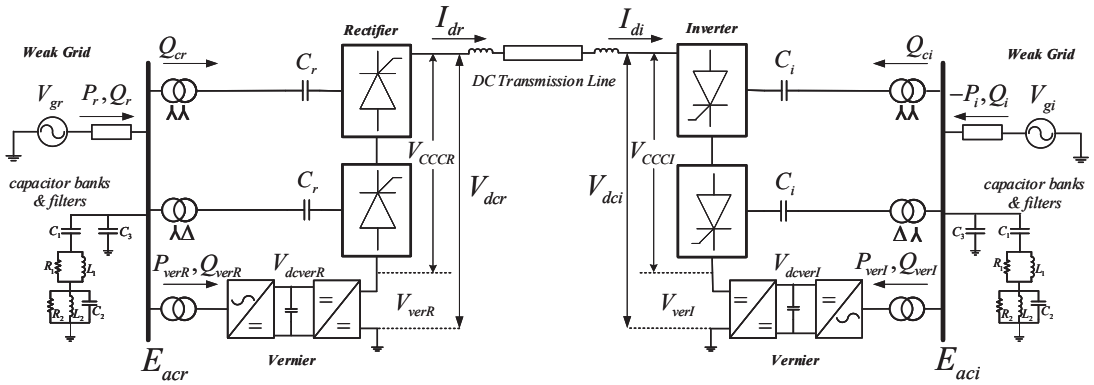

Fig. 1. Hybrid-HVDC system.

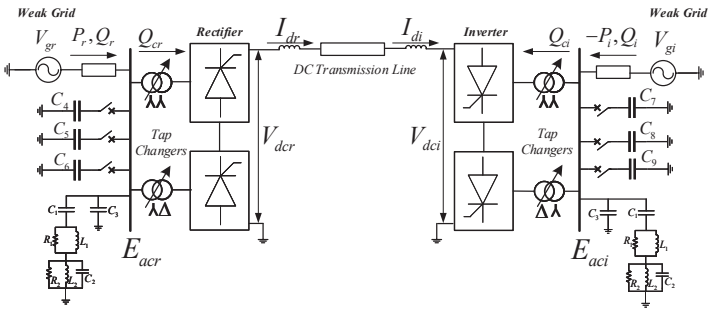

Fig. 2. LCC-HVDC system.

K_{iDC} in addition to the volt-VAr control of the commutating bus through controller gains K_{pQ}, K_{iQ}, K_{pV} and K_{iV}. Traditional vector control with inner current control loops are employed. The volt-VAr control forms a cascaded structure with a slow reactive power tracking loop generating an AC voltage reference E^*_{acr} for a faster voltage regulation loop, see Fig. 5.

□ *Steady State Behavior:* The CCC operates with the minimum firing angle $\alpha^*_r = \alpha^*_{r\_min} = -16deg$. Assuming V_{dcverR} is tightly controlled, Δ_{bleedr} is also zero. This ensures that the steady state Vernier voltage is a pre-designed fraction K_{verR} of the commanded total voltage integral, i.e., $V_{verR} = K_{verR} \int dV^*_{dcr}$. Under nominal condition $V_{verR} > 0$ and when V_{verR} goes into saturation, control over α_r is lost.

To minimize the AC-DC converter current in the Vernier, Q^*_{verR} is usually set to zero, see Fig. 5. When E^*_{acr} goes outside the pre-determined voltage regulation limits of V_{max} and V_{min}, the VAr regulation loop loses control and the Vernier supplies nonzero steady-state Q_{verR} to regulate the voltage at one of the limits V_{max} or V_{min}, whichever is hit. Note that scenarios where the AC voltage hits the saturation limits is likely to occur during large transient disturbances. In such condition the control will not allow AC voltage to go outside V_{max}/V_{min}. When the transient event passes, the voltage comes back within the limits and the VAr control becomes active again.

□ *Dynamic Behavior:* During dynamic condition, the coordinating control goes through the following sequence of events:

- The value of V^*_{dcr} starts changing, which alters V^*_{CCCR} and V^*_{verR}. The change in V^*_{CCCR} changes firing angle command α^*_r. If $\alpha^*_r > \alpha^*_{minr}$, reactive power consumed by CCC increases.
- The vernier voltage command V^*_{verR} changes following equation (2) to drive α^*_r to its pre-disturbance minimum value. $K_{\alpha r}$ determines how fast α^*_r returns to $\alpha^*_{r\_min}$.
- To avoid frequent limit hitting, the minimum value of V^*_{dcr} is adaptively changed as a function of V_{dcr} (Fig. 3).
- For Vernier's AC-DC converter (Fig. 4), the limits on the $q-$axis current is dynamically adjusted. As shown in Fig. 5, the $d-$axis current is given higher priority and the limits on the $q-$axis current is determined using the headroom $\sqrt{(I_{max})^2 - (I^*_{dver})^2}$, where I_{max} is the converter current rating.
- If the Vernier DC-link voltage V_{dcverR} reduces below a threshold due to limit hitting in the $d-$channel, it can drive the duty cycle of Vernier's DC-DC converter (Fig. 4) to saturation. To avoid this, a bleeder scheme acts based on a lookup table, see Fig. 3, which produces a -ve output Δ_{bleedr} to reduce V^*_{verR} in equation (2).

B. Inverter-side Control

The inverter-side control is shown in Fig. 6, which consists of a CC loop and a DC voltage control (VC) loop. As shown in Fig. 6, the control laws can be described as:

$$\begin{aligned} V_{cmdi\_VC} &= K'_{pi}\left(V^*_{di} - V_{dci}\right) + K'_{ii}\int\left(V^*_{di} - V_{dci}\right)dt \\ V_{cmdi\_CC} &= -K_{pi}\left(I^*_{dr} - I_{di} - I_{margin}\right) \\ &\quad - K_{ii}\int\left(I^*_{dr} - I_{di} - I_{margin}\right)dt \end{aligned} \tag{3}$$

In normal condition, the rectifier operates in CC mode, which drives the output of the inverter CC loop to V_{cmdi_max}. Therefore, the inverter operates in VC mode, which produces a control command V^*_{dci} corresponding to the total DC voltage at the inverter-end. Under certain conditions, the rectifier might loose control over the current (if α^*_r hits limit) and the inverter CC loop might become active. As shown in Fig. 3, V^*_{dci} is split between the CCC and the Vernier:

$$\begin{aligned} V^*_{dci} &= \min\left\{V_{cmdi\_CC}, V_{cmdi\_VC}\right\} \\ V^*_{dci} &= V^*_{CCCI} + V^*_{verI} \end{aligned} \tag{4}$$

The Vernier voltage reference is synthesized using the following relationship:

$$V^*_{verI} = K_{verI}\int dV^*_{dci} + K_{\gamma i}\int\left(\gamma^*_{i\_\min} - \underbrace{\min}_{of12}\left\{\gamma_i\right\}\right)dt - \int \Delta_{bleedi}dt \tag{5}$$

where, $\min_{of12}$ indicates the minimum of the 12 thyristors in the 12-pulse bridge. Also, Δ_{bleedi} is the output of a bleeder scheme, which is -ve (+ve) if the DC-link voltage V_{dcverI} of the Vernier shown in Fig. 1 falls below (goes above) a threshold. The AC-DC converter of the Vernier is controlled in the same manner as described for the rectifier-side.

□ *Steady State Behavior:* The CCC operates with the margin angle $\gamma_i = \gamma^*_{i\_min} = 17deg$. Assuming V_{dcverI} is tightly

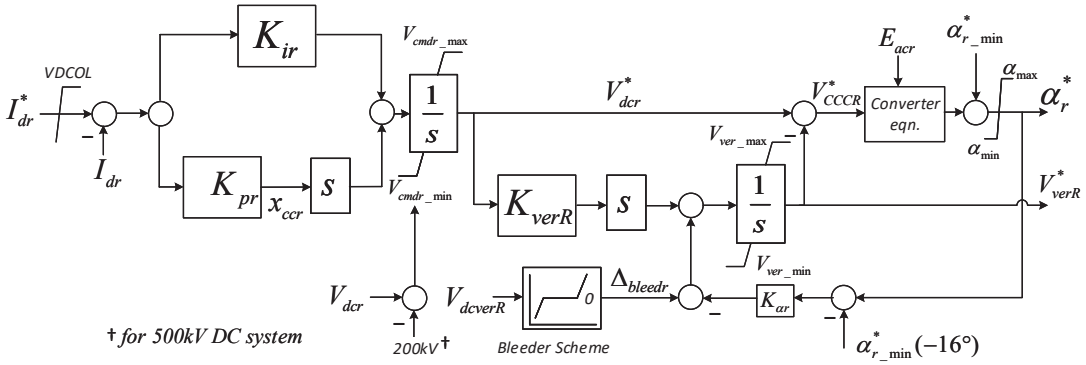

Fig. 3. Proposed rectifier-side coordinating control.

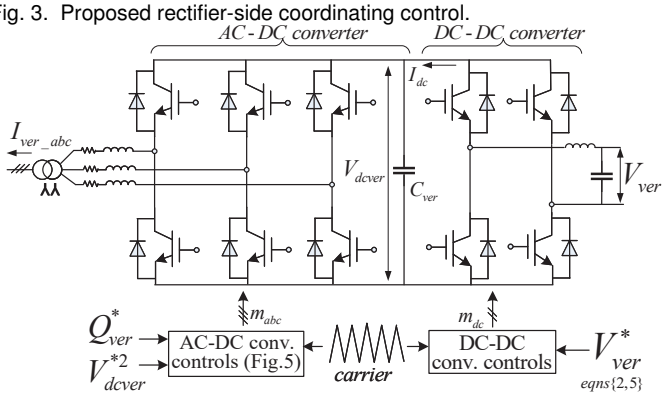

Fig. 4. Single unit of Vernier converter topology used in present work.

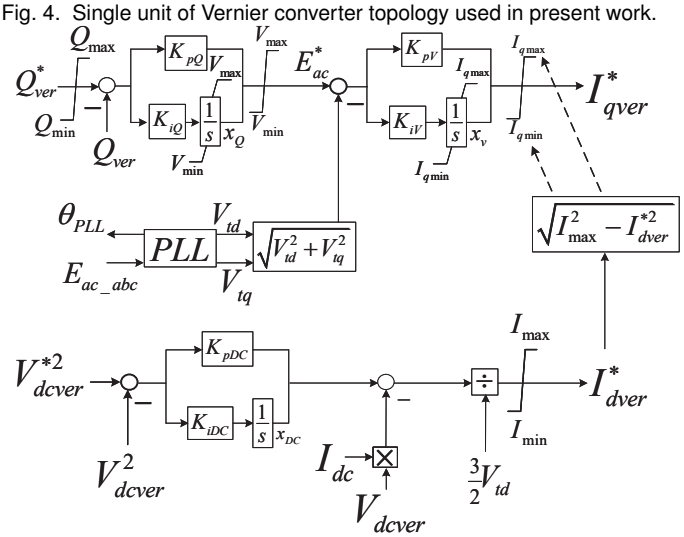

Fig. 5. Vernier AC-DC converter controls (rectifier and inverter-side): Outer reactive power control loop, AC voltage control, DC-link voltage control, and current limiting strategy.

controlled, Δ_{bleedi} is zero. This ensures that the steady state Vernier voltage is a pre-designed fraction K_{verI} of the commanded total voltage integral, i.e., $V_{verI} = K_{verI} \int dV^*_{dci}$. Under nominal condition, $V_{verI} < 0$ and when V_{verI} goes into saturation, control over α_i is lost.

□ *Dynamic Behavior:* The dynamic behavior of the coordinating control is similar to that of the rectifier-end. To avoid frequent limit hitting, the maximum value of V^*_{dcr} is adaptively changed using a function of V_{dci} (Fig. 6).

V. Proposed State-Space Averaged Model

In this section, the nonlinear state-space averaged phasor model of the Hybrid-HVDC system mentioned above is derived in the form of Differential and Algebraic Equations (DAEs). The main components of this system are CCC and the Vernier, which are modeled below:

A. Capacitor Commutated Converter (CCC)

The modeling of CCC involves transcendental equations, which are mentioned in literature [18], [19]. However these papers did not consider capacitor dynamics and the effect of unbalance in capacitor voltages. This issue was reported by W. Hammer in [25], but an oversimplified algebraic model of CCC was considered in this work, which is not suitable for representing the inverter. Therefore, it was tested only on the rectifier-end of a CCC-HVDC system where the inverter was modeled using a voltage source. In contrast, this paper has included the capacitor dynamics and the effect of unbalance in capacitor voltages along with the detailed algebraic model of CCC. The algebraic model of CCC [18], [19] is expressed as follows:

$$u_{do} = \frac{3\sqrt{2}}{\pi}\frac{V_{ss}}{Tap};\ d_{xl} = \frac{3\omega L_c}{\pi};\ d_{xc} = \frac{2}{\pi\omega C};\ \omega_o = \sqrt{\frac{d_{xc}}{d_{xl}}};$$
$$u_{cN} = \frac{\pi^2 d_{xc}}{9};\ K = \frac{1}{2}\frac{1}{(d_{xc}-d_{xl})}; E = K u_{do}\cos(\alpha) - \frac{I_d}{2}$$
$$F = K u_{do}\omega_o \sin(\alpha) + \frac{\pi\omega_o}{3} I_d - \frac{3\omega_o}{2\pi d_{xc}\omega}\Delta V_1$$
$$\beta = \arctan\left(\frac{F}{E}\right), \quad -\pi < \beta < \pi; \qquad Y = \sqrt{E^2+F^2} \tag{6}$$

$$\Delta V_1 = \frac{2\pi d_{xc}}{3\,(1+\cos(\omega_o\mu))}\left[\frac{I_d\mu}{2} - K u_{do}\sin(\alpha+\mu) + \frac{1}{\omega_o}\left(K u_{do}\cos(\alpha)+\frac{I_d}{2}\right)\sin(\omega_o\mu) + K u_{do}\sin(\alpha)\cos(\omega_o\mu) + \frac{\pi}{3} I_d\,(\cos(\omega_o\mu)-1)\right] \tag{7}$$

$$\frac{-\pi}{3}u_{do}\sin(\alpha+\mu+\gamma_i) - 2u_{cN}I_d - \Delta V_1 + \frac{\pi d_{xc}}{3} I_d(\mu+\gamma_i) = 0 \tag{8}$$

$$V_d = u_{do}\frac{\cos(\alpha+\mu)+\cos(\alpha)}{2} + \left(1-\frac{3}{4\pi}\mu\right)(2\Delta V_1 - \frac{\pi}{3} I_d \mu d_{xc}) \tag{9}$$

$$\frac{I_d}{2} - K u_{do}\cos(\alpha+\mu) - Y\cos(\omega_o\mu - \beta) = 0 \tag{10}$$

where, u_{do}: no-load direct voltage; V_{ss}: phase-to-phase voltage of the valve-side of the converter transformer; I_d: DC current; α: firing angle relative to AC bus voltage; μ: overlap angle; C: capacitance of the commutation capacitor; ω: system frequency (in pu); L_c: transformer leakage inductance; ΔV_1: changes in capacitor voltages during commutation for outgoing valve; γ_i: commutation margin defined as the angle between the end of commutation interval and the valve voltage positive zero crossing. Each variable in Eq. (6) is converted to

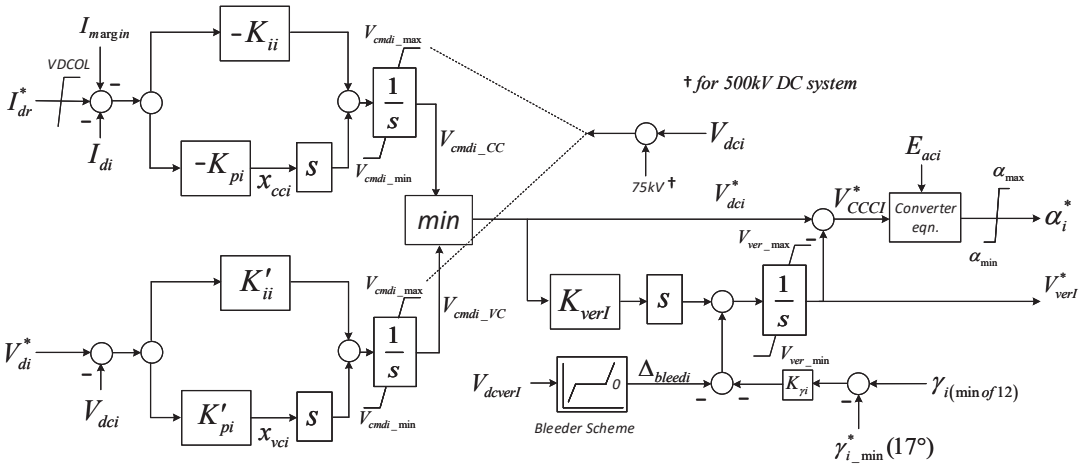

Fig. 6. Proposed inverter-side coordinating control.

per unit per bridge, considering the valve-side voltage of the transformer as the base voltage.

The apparent power consumed by the converter can be written as:

$$S = P + jQ = 3U_1 I_1^* \tag{11}$$

where, U_1 is the fundamental-frequency rms phase-to-ground voltage and I_1 the fundamental-frequency rms AC line current at the valve-side of the transformer. Considering the phase angle of U_1 as reference, the relationships between U_1, I_1, and the DC variables are given by:

$$U_1 = \frac{\pi}{3\sqrt{6}} u_{do} \tag{12}$$

$$I_1 = \frac{\sqrt{6}e^{-j\alpha}}{\pi}\left\{\frac{I_d}{2}(1+e^{-j\mu}) + \frac{K u_{do}}{2}\left[\frac{e^{-j\alpha}}{\pi}(1-e^{-j2\mu}) + j\mu e^{j\alpha}\right] + \frac{Y}{\omega_o^2-1}\left[e^{-j\mu}\{\cos(\omega_o\mu-\beta) + j\omega_o\sin(\omega_o\mu-\beta)\} - \cos(\beta) + j\omega_o\sin(\beta)\right]\right\} \tag{13}$$

The dynamics of capacitor is included by considering two real differential equations in terms of real and imaginary part of the averaged space-vector of the fundamental frequency component of commutation capacitor voltage, $\vec{v}_C^{(1)}$, i.e., $\Re(\vec{v}_C^{(1)})$ and $\Im(\vec{v}_C^{(1)})$, respectively, [25]:

$$\begin{aligned}\Re(\dot{\vec{v}}_C^{(1)}) &= -\frac{1}{C}\Re(\vec{i}^{(1)}) + \omega\Im(\vec{v}_C^{(1)}) \\ \Im(\dot{\vec{v}}_C^{(1)}) &= -\frac{1}{C}\Im(\vec{i}^{(1)}) - \omega\Re(\vec{v}_C^{(1)})\end{aligned} \tag{14}$$

The average contribution of the unbalance in capacitor voltages to the direct voltage [25] is given as:

$$\Delta V_{d,C} = \frac{\pi^2}{6}\left|\vec{v}_C^{(1)}\right|\cos(\arg(\vec{v}_C^{(1)}) - \arg(\vec{i}^{(1)})) \tag{15}$$

This contribution is added to the DC-side voltage mentioned in Eq.(9).

B. Vernier

The vernier is modeled using power balance equations while its control has been explained in Section IV. The power consumed by the vernier from PCC (see, Figs 1 and 4) can be expressed as:

$$S_{ver} = P_{ver} + jQ_{ver} = -\sqrt{3}E_{ac}I_{ver}^* \tag{16}$$

Unity power factor is maintained through the Vernier controls mentioned before. Neglecting converter losses. the real power balance equation with the DC sides of the AC-DC and DC-DC converters can be expressed as (Figs 1, 4):

$$P_{ver} - \frac{1}{2}C_{ver}\frac{dV_{dcver}^2}{dt} = -I_{dc}V_{dcver} = \pm I_d V_{ver}, \tag{17}$$

where +ve and -ve signs in the rightmost term are applicable for the rectifier and the inverter Vernier, respectively. Apart from CCC and vernier, the other components of the system are the DC-line and the AC network, which are modeled as mentioned in [26]. The interconnection of these components in the nonlinear state-space averaged model of the Hybrid system is shown in Fig. 7. Here the rectifier/inverter include both the CCC and vernier models.

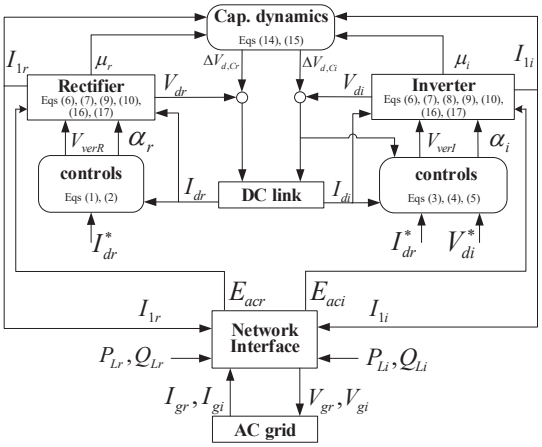

Fig. 7. Block diagram representing nonlinear dynamic model of Hybrid-HVDC system.

Remark: *The main application of the derived analytical (state-space averaged) model is frequency-domain analysis, which helps in understanding the root-cause of dynamic behavior of the system. The other application is control parameter selection and controller design.* ***Note that none of these can be performed by the detailed PSCAD model.***

VI. Modal Analysis, Controller Design & Benchmarking of Averaged Model

A. Test system

The test system in Fig. 1 considers two weak 345-kV AC grids connected to the rectifier and the inverter stations whose individual Short Circuit Ratio (SCR) is 2.5. The impedance characteristic of the two grids are identical. The Vernier voltage rating is 40kV, which is less than 10% of the CCC voltage

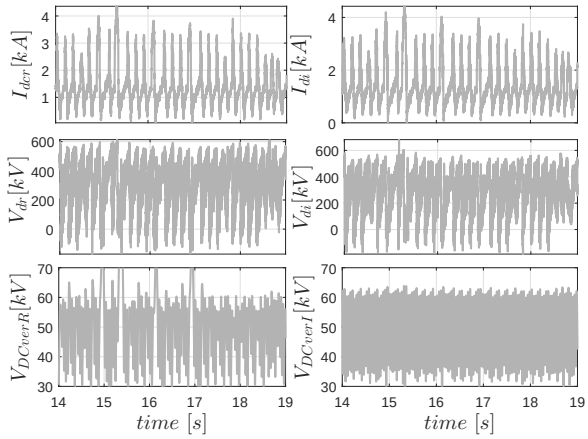

Fig. 8. Response of the detail switched model of test system in EMTDC/PSCAD.

TABLE II
CRITICAL MODES CAPTURED BY THE PROPOSED AVERAGED MODEL

$\xi, \%$	-2.29	-2.18	0.51	0.33	0.88
f, Hz	29.25	30.177	50.318	69.59	84.062

rating of $500kV$. Each vernier unit (see, Fig. 4) has a DC bus voltage (V_{dcver}) rating of 1.4 kV - one such unit is represented using a detailed model and the others using a functional model. A 1000-km long 500kV DC transmission line is considered, which is represented by a Bergeron model. The modeling and analysis are performed in EMTDC/PSCAD software [27]. The details of the system parameters are mentioned in the Appendix.

B. Time-domain response in EMTDC/PSCAD

The response of the system with initial values of Vernier controller gains as $K_{pDC} = 2.4 \times 10^{-4}$, $K_{iDC} = 9.0$, $K_{pQ} = 0.01$, $K_{iQ} = 0.10$, $K_{pV} = 0.02$, $K_{iV} = 2.37$ is shown in Fig. 8. It can be seen that the system is unstable. To find the root-cause of the dynamic performance of the system the proposed averaged model is used.

C. Modal analysis for controller design

The proposed averaged model is linearized around the operating point to check the unstable modes in the system. Table II shows two unstable modes of frequency $29.25Hz$ and $30.17Hz$ captured by the linearized model. After finding the unstable modes, the following approach is considered:

Eigenvalue-sensitivity analysis: Eigenvalue-sensitivity analysis was performed to examine the effect of variation of controller parameters on the unstable modes. The 1^{st}-order eigenvalue sensitivity is given as [28]:

$$\boxed{\frac{\partial \lambda_i}{\partial \Gamma} = \frac{\psi_i \frac{\partial A}{\partial \Gamma} \phi_i}{\psi_i \phi_i}} \tag{18}$$

where, Γ is a system parameter (in this case Vernier's controller gains). The sensitivity was approximated by $\frac{\psi_i \frac{\Delta A}{\Delta \Gamma} \phi_i}{\psi_i \phi_i}$, where ΔA denotes the change in the state-matrix corresponding to a small change in parameter Γ. Table III shows the eigenvalue sensitivity with respect to the Vernier controller gains. Following are the observations:

- The eigenvalue-sensitivity is computed by reducing the Vernier's controller gains. Therefore, a positive $\frac{\partial \sigma_i}{\partial \Gamma}$ indicates the real part of the eigenvalue is moving towards left and a positive $\frac{\partial \omega_{di}}{\partial \Gamma}$ indicates a reduction of the value ω_{di}.
- Among all the controllers, both the unstable modes have highest sensitivity with respect to the DC-link voltage controller gain K_{pDC} (highlighted in Table III).
- With the reduction in K_{pDC} the real part is moving towards right, making these modes more unstable, along with decrease in modal frequency. However, there are insignificant changes with respect to the other controller parameters.

Root locus analysis: The Vernier DC-link controller parameter K_{pDC} is tuned using root-locus method while utilizing the eigenvalue sensitivity information from the previous step. Figure 9 shows the eigenvalue movement with increase in K_{pDC} value to 500 times of the nominal value. Both the unstable modes are stabilized with increase in K_{pDC} to 0.12.

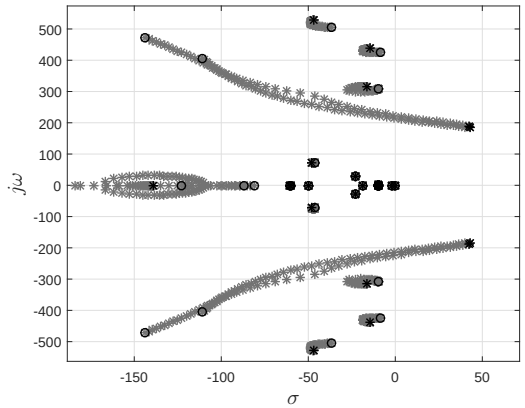

Fig. 9. Eigenvalue-movement with increase in Vernier's DC-link controller gain (K_{pDC}) from 2.4×10^{-4} to 0.12.

D. Benchmarking of Averaged Model

The system is stabilized with the appropriate selection of K_{pDC} (0.12) from the previous step. In the current operating condition, $1010MW$ power is transmitted from the rectifier end while reactive power of $-300MVAr$ is consumed. The inverter receives nearly $940MW$ and consumes reactive power of $-180MVAr$. The current order is $2kA$ with the combined DC voltage (CCC and Vernier) of $500kV$ at the rectifier end.

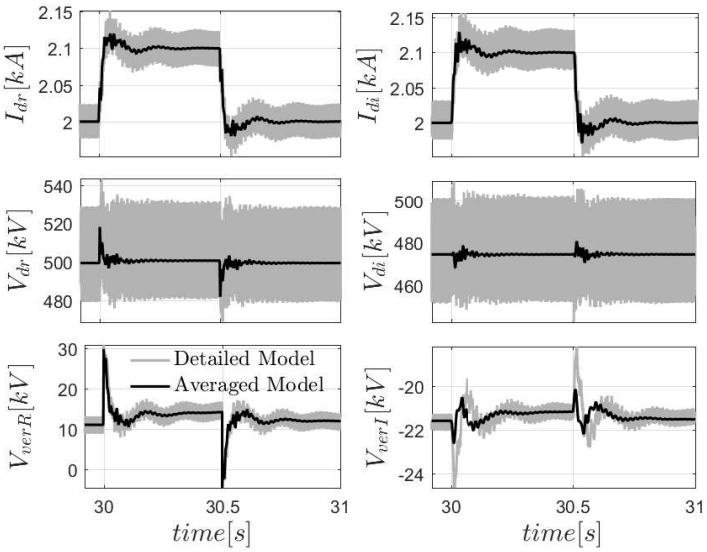

Fig. 10. Dynamic response of the system following a pulse-increase in the current reference of the rectifier current controller.

TABLE III
EIGENVALUE SENSITIVITY ANALYSIS FOR WEAK SYSTEM: SCR =2.5, NOMINAL VALUES $K_{pDC} = 2.4 \times 10^{-4}$, $K_{iDC} = 9.0$, $K_{pQ} = 0.01$, $K_{iQ} = 0.10$, $K_{pV} = 0.02$, $K_{iV} = 2.37$ $\Delta\Gamma < 0$, I.E. PARAMETERS WERE REDUCED

Modes $\lambda_i = \sigma_i \pm j\omega_d$	$\frac{\partial\sigma_i}{\partial\Gamma}$						$\frac{\partial\omega_{di}}{\partial\Gamma}$					
	K_{pDC}	K_{iDC}	K_{pQ}	K_{iQ}	K_{pV}	K_{iV}	K_{pDC}	K_{iDC}	K_{pQ}	K_{iQ}	K_{pV}	K_{iV}
$42.36 \pm j189.61$	-1476.6	3.99	2.08	-0.003	-6.06	-0.052	1124.9	8.68	-1.11	-0.012	-9.07	0.020
$43.27 \pm j183.81$	-1364.5	3.48	0.40	0.006	4.78	-0.006	996.4	8.24	1.11	-0.000	-2.32	-0.03

TABLE IV
MODAL PARTICIPATION ANALYSIS OF HYBRID SYSTEM (SCR = 2.5)

Dominant States	$\lambda_i = \sigma_i \pm j\omega_{di}$
I_{dr}, I_{di}, $\Re(\vec{v}_{Ci}^{(1)})$, $\Im(\vec{v}_{Ci}^{(1)})$, $\Re(\vec{v}_{Cr}^{(1)})$, V_{dm}	$-35.405 \pm j505.232$
$\Re(\vec{v}_{Ci}^{(1)})$, $\Im(\vec{v}_{Ci}^{(1)})$, $\Re(\vec{v}_{Cr}^{(1)})$, $\Im(\vec{v}_{Cr}^{(1)})$	$-8.093 \pm j425.320$
$\Re(\vec{v}_{Ci}^{(1)})$, $\Im(\vec{v}_{Ci}^{(1)})$, $\Im(\vec{v}_{Cr}^{(1)})$, V_{dm}	$-9.384 \pm j309.453$

Figure 9 shows the dynamic response of the detailed switched model in PSCAD and proposed analytical model in MATLAB following a pulse-increase in the current reference of the rectifier current controller from $2kA$ to $2.1kA$, which excites the CCC and vernier dynamics. The close match between their responses validates the accuracy of the state-space averaged model.

E. Modal analysis in a progressively weak system

After gaining confidence in the accuracy of the averaged model, in this section a deeper understanding of the system dynamics is developed through modal analysis with the decrease in SCR of the system. Root-locus analysis was performed starting from the strong system ($SCR = 24.6$) to observe the eigenvalue movement as the system is made progressively weaker by gradual reduction in SCR up to 1.97. Figure 11, shows the movement of the modes as the SCR is reduced. The states participating in the modes that are responsible for negatively influencing system stability as the grid become weaker are determined using participation factor analysis [28]. In Table IV, the states having maximum participation in the modes with frequencies $80.4Hz$, $75.3Hz$, and $49.2Hz$, which are very sensitive to reduction in SCR and moving towards the right half in Fig. 11 are identified.

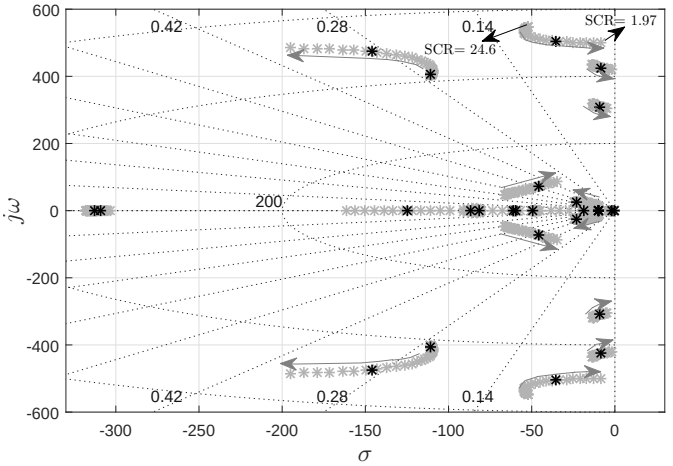

Fig. 11. Eigenvalue-movement with reduction in SCR that makes the AC grid progressively weaker.

VII. STEADY-STATE OPERATIONAL CHARACTERISTICS

The steady-state operational characteristics of the Hybrid HVDC system with change in loading and AC system voltages

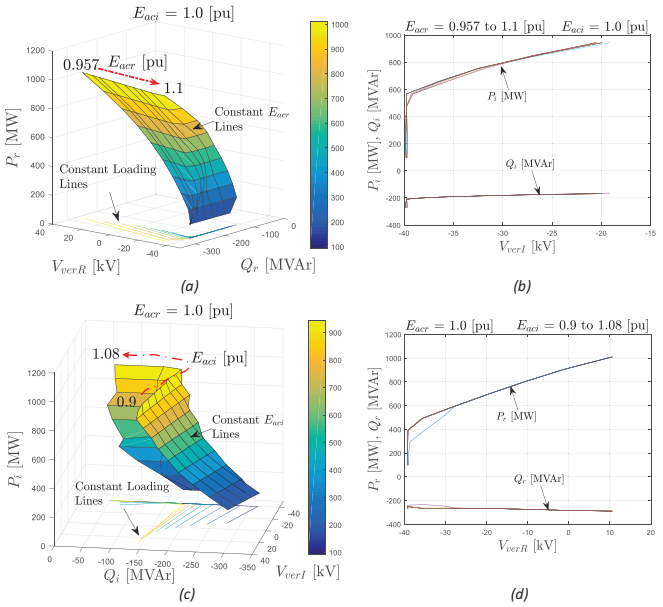

Fig. 12. Steady state operational characteristics of the Hybrid HVDC system with change in loading. When E_{acr} is varied and E_{aci} is kept constant: (a) rectifier and (b) inverter characteristics. When E_{aci} is varied and E_{acr} is kept constant: (c) inverter and (d) rectifier characteristics.

are obtained from the detailed PSCAD model and are shown in Fig. 12. The change in loading is achieved by modifying the value of I_{dr}^*. For each loading condition, the values of the rectifier-side AC voltage E_{acr} is varied between 0.96 to 1.1pu while keeping the inverter-side AC voltage E_{aci} constant at 1.0pu. Figures 12(a) and (b) show the rectifier and inverter characteristics, respectively. Similarly, when E_{aci} is varied from 0.9 to 1.08pu and E_{acr} is kept constant at 1.0pu; the inverter and rectifier characteristics are shown in Figs 12(c) and (d), respectively. The following observations can be made from these characteristics:

1. Constant E_{acr} (E_{aci}) lines in Figs 12(a) and (c) indicate that unless the AC voltage is too close to 1.1pu, the Vernier operates within its limits of $\pm$40kV. The constant loading lines indicate that unless the power flow is as small as 40% of the rated value, Vernier operates without saturation.

2. When Vernier output is not saturated (Figs 12(a), (c)), variations in Q_r and Q_i are insignificant compared to those of P_r and P_i. When V_{ver} hits its lower limit, these variations increase. However, it is highly unlikely that the AC grids will operate under a steady state voltage in the vicinity of 1.1pu along with loading as low as 40%.

3. The operating characteristics of the inverter (rectifier) with change in loading condition is nearly independent of the variation in AC voltage at the rectifier (inverter) end, see Figs 12(b) and (d). As expected, the reactive power consumption of the converter stations remain practically constant over the

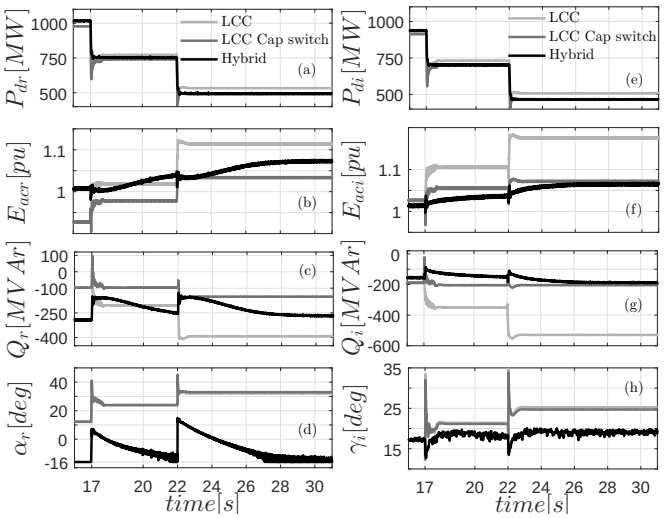

Fig. 13. Comparison of dynamic behavior of LCC HVDC and Hybrid HVDC following a step reduction in current order I^*_{dr} from 1.0pu to 0.75pu at $t = 17.0$s followed by a further reduction to 0.50pu at $t = 22.0$s. The variables are marked in Figs 1 and 2.

operating range.

VIII. Dynamic Performance in Weak AC System: LCC vs Hybrid

The dynamic performance of the Hybrid HVDC is compared with the LCC HVDC system, while keeping the same weak AC systems described in section VI-A for both cases. To ensure similar boundary conditions under rated load in terms of the rectifier and inverter commutating bus voltages, additional shunt capacitor banks are needed for LCC stations. Under nominal condition, the values of α_r and γ_i for the CCC in Hybrid scheme are -16deg and 17deg, respectively. The corresponding values for the LCC stations are 20deg and 17deg, respectively. The LCC system is controlled following the philosophy described in the Cigre' benchmark model [29]. Figures 2 and 1 show the filters and capacitor banks used for the Hybrid and the LCC stations.

A. Step Reduction in Power Flow

To demonstrate the effectiveness of the proposed coordinating controller described in section IV, the current order I^*_{dr} in the rectifier is reduced in two steps. At $t = 17.0s$, the current order is reduced to 75% of the rated value followed by a further reduction to 50% of its rated value at $t = 22.0s$.

Figure 13 shows the dynamic behavior when no capacitor bank switching takes place in LCC, and when capacitor banks are switched out. At the rectifier-side $C_4 = 1.7$uF and $C_5 = 1.5$uF are switched out at $t = 17.0$s and $t = 22.0$s, respectively. The corresponding values for the inverter-end are $C_7 = 2.05$uF and $C_8 = 2.15$uF, respectively. From these figures, the following observations can be made:

1. LCC HVDC: Reduction in loading leads to a reduction of reactive powers Q_{cr} and Q_{ci} demanded by the converters. When the shunt capacitors are not switched out, this leads to a significant increase in net reactive power supplied by the stations Q_r and Q_i, which causes a significant increase in E_{acr} and E_{aci}. In practice, shunt capacitor banks are switched out following a reduction in loading. As shown in Figs 13(b) and 13(f), this significantly improves the AC voltage profiles

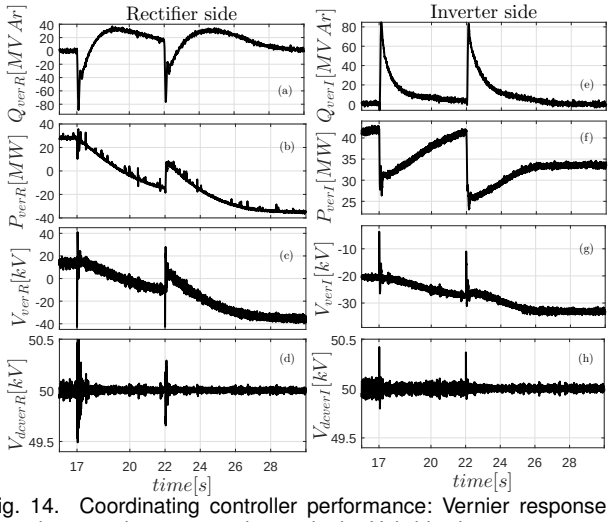

Fig. 14. Coordinating controller performance: Vernier response with step decrease in current order I^*_{dr} in the Hybrid scheme.

since the change in net reactive power Q_r and Q_i becomes much lesser. Such operations increase the complexity of the switchyards - please see Fig. 2 to compare with the Hybrid scheme in Fig. 1.

2. Hybrid HVDC: Figure 13 shows the response of the Hybrid scheme while Fig. 14 shows the Vernier response. These figures illustrate the effectiveness of the proposed coordinating controller described in section IV.

With step decrease in current, the values of α_r and γ_i changes, which increase the net reactive power Q_r and Q_i demanded by the CCC station (became less negative). As shown in Fig. 14(c), the coordinating control slowly reduces the rectifier-side Vernier voltage and drives it into a negative polarity, which brings α_r back to the pre-disturbance value. This also brings the net reactive power consumption Q_r very close to the pre-disturbance value, see Fig. 13(c). The reactive power Q_{verR} contributed by the Vernier is reduced to zero (Fig. 14(a)) by the slow outer loop shown in Fig. 5. Note that the values of V_{max} and V_{min} chosen in Fig. 5 are 1.1pu and 0.9pu, respectively. Since E_{acr} remains within this range, the reactive power control loop of the Vernier remains operational. Similar observations can be made on the response of the coordinating control in the inverter-side.

The Vernier DC-link voltages V_{dcverR} and V_{dcverI} are tightly controlled, see Figs 14(d) and (h). As observed, the proposed coordinating control in Hybrid HVDC performs acceptably without any need for switched capacitors or tap changers.

B. Severe Fault Scenarios

In this section, the performance of Hybrid HVDC is compared against that of LCC HVDC following severe faults. Specifically, two aspects of system performance (1) power flow recovery and (2) commutation failure have been considered.

Three-phase inverter-side fault: Figure 15 shows the dynamic performance following a three-phase bolted fault for 5 cycles at $t = 19.99s$ on the inverter commutating bus. This is considered to be the most severe fault, especially in presence of a weak system on the AC side. As Fig. 15 shows, LCC is not able to recover the power within the specification of $300ms$. Moreover, a severe commutation failure occurs in LCC during

fault, while in case of Hybrid topology, the commutation failure is significantly reduced compared to LCC. Also, the Hybrid system recovers power transmission within 90% of the pre-fault steady-state value within $220ms$.

DC-side fault: A zero-impedance DC fault at the rectifier terminal is considered at $t = 20.0s$, which momentarily causes the rectifier current to increase and inverter current to decrease. Considering the detailed literature on the DC fault detection and protection [30]–[38], it is assumed that the fault is detected in $1ms$- typical for VSC HVDC systems. The fault current is extinguished using the process called "forced retard". In this process, the inverter is kept in inversion mode - for Hybrid case the inverter firing angle α is reduced to $140deg$ whereas the β value for LCC is limited to $80deg$, see Fig. 16(i). At the time of detection the rectifier is driven to inversion mode by increasing the firing angle to $100deg$ for the Hybrid system and $140deg$ for the LCC. *It can be seen from Fig. 16(a) that the peak value of current in the hybrid system is nearly* $1.75pu$ *for less than* $5ms$*. Similar to the standard practice in VSC HVDC, we propose that the IGBT modules can be bypassed by press-pack thyristors and contactors to provide protection against surge current as described in [38].* The fault current is extinguished within $40ms$ of initiating "forced retard" and the valves are blocked at $t = 20.04s$. After allowing $500ms$ time to de-ionize the overhead lines, the valves are de-blocked.

In this case as well, Hybrid system performs better than LCC-HVDC. As shown in Fig. 16(j), the LCC system goes through commutation failure following the converter de-blocking and it is not able to meet the power recovery specification.

Figure 17 shows the performance of the Vernier following different above mentioned faults. The DC voltage injected by the inverter-side Vernier during three-phase self-clearing fault at the inverter-side is shown in Fig. 17(a), whereas Fig. 17(c)

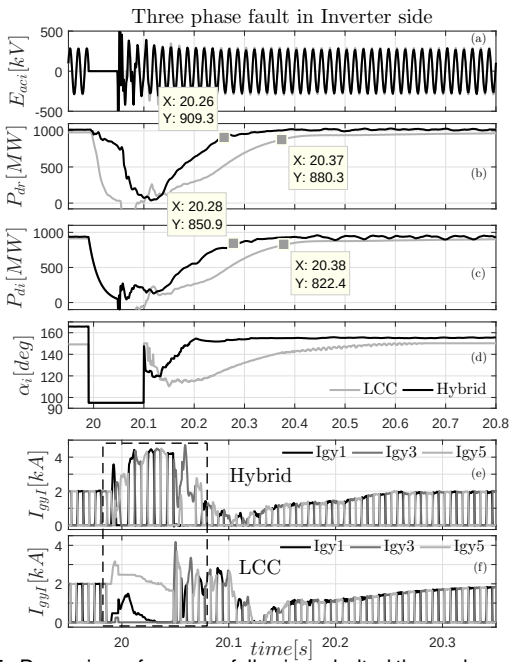

Fig. 15. Dynamic performance following a bolted three-phase fault at the phase zero-crossing of the commutating bus voltage in the inverter-side at $t = 19.99s$ for 5 cycles.

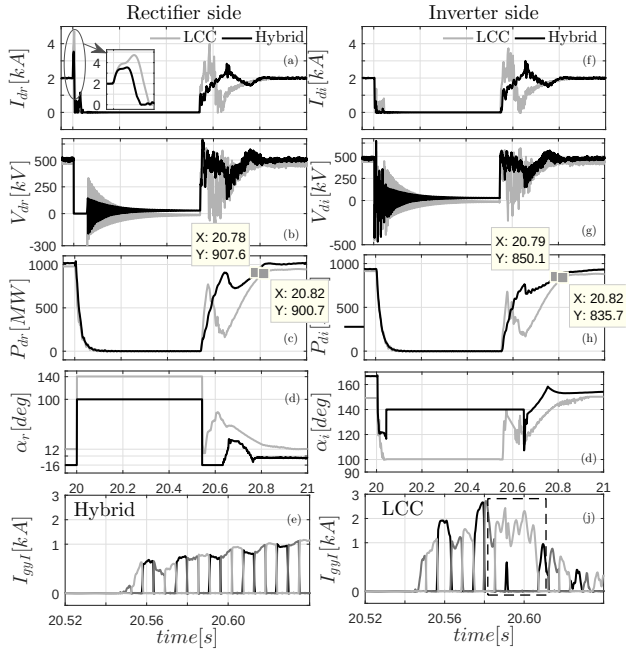

Fig. 16. DC Fault response considering fault detection time of 1ms. The peak value of current in Hybrid HVDC is nearly 1.75 pu for less than 5ms.

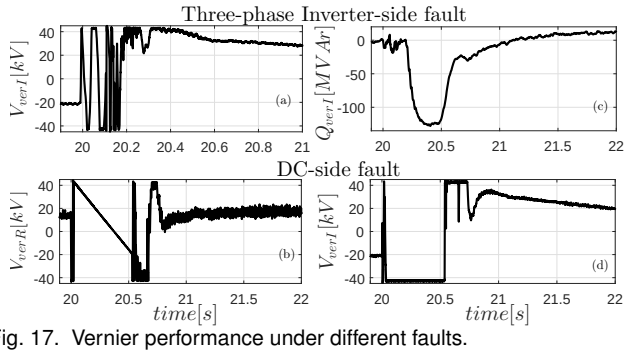

Fig. 17. Vernier performance under different faults.

shows the VAr support provided by the Vernier following this fault and then the slower outer loop shown in Fig. 5 brings it back to zero. The variation in the rectifier and inverter-side Vernier voltages doe the DC fault case are shown in Figs 17(b) and (d).

IX. Conclusion

This paper attempted to fill the gap in Hybrid HVDC literature by proposing a control strategy, which can ensure coordination between a Capacitor Commutated Converter (CCC) and a 2-stage Voltage Source Converter (VSC) called 'Vernier'. To that end, the characteristics of this Hybrid system was established. It was shown that the Vernier can maintain practically constant reactive power consumption by the CCC over a wide range of loading conditions. Moreover, a nonlinear state-space averaged modeling framework for the proposed system has been developed for the frequency-domain analysis of progressively weak AC grid. This model is benchmarked against a detailed switched model. The states which can make the system unstable when AC grid further becomes weak have been identified through small-signal stability analysis. Also, effectiveness of the proposed strategy in terms of recovery of

power flow and commutation failure following severe disturbances is demonstrated through time-domain simulations.

X. Appendix

A. Hybrid-HVDC parameters:

$R_L = 12.5\ \Omega$, $L_{dc} = 1.4515\ H$, $L_c = 0.12\ (pu)$,
$C_{dc} = 13.6\ \mu F$, $C_1 = 2.217\ \mu F$, $R_1 = 2000\ \Omega$,
$L_1 = 0.00979\ H$, $R_2 = 500\ \Omega$, $L_2 = 0.00535\ H$,
$C_2 = 5.1329\ \mu F$, $C_{3r} = 3.2\ \mu F$, $C_{3i} = 4.2\ \mu F$,
$C_r\ = C_r\ = 112\ \mu F$

TABLE V
HYBRID HVDC SYSTEM

AC Side		DC Side	
Rated power	$1000\ MVA$	DC voltage	$500\ kV$
Grid voltage	$345\ kV$	DC current	$2\ kA$
Transformer ratio	$345/182\ kV$	DC cable length	$1000\ km$
Transformer rating	$557MVA$		

B. Key variables of the proposed averaged model

State variables (x): $I_{dr},\ x_{ccr},\ x_{vR},\ x_{Qr},\ x_{DCr},\ V_{dm},\ V^*_{verR},$
$I_{di},\ x_{cci},\ x_{vci},\ x_{vI},\ x_{Qi},\ x_{DCi},\ V^*_{verI}$
Algebraic variables (z): $V_{ssr},\ \mu_r,\ Tap_r,\ V_{ssi},\ \mu_i,\ Tap_i,\ \gamma^*_i$
Input variables (u): $\alpha_r,\ V_{verR},\ \alpha_i, V_{verI}$

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