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ELECTRICAL AND THERMAL LAYOUT DESIGN AND OPTIMIZATION CONSIDERATIONS FOR DPS ACTIVE IPEM

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ABSTRACT

A methodology was developed to optimize the 3D geometrical design layout of an active integrated power electronics module (IPEM) by considering both electrical and thermal performance. This paper is focused on the thermal analysis, which was performed using 3D finite element and computational fluid dynamic (CFD) analyses. A parametric study was conducted to determine the thermal performance of several different design layouts. A sensitivity analysis was performed to determine the overall uncertainty of the predicted simulations. The final design, Gen-II.C, provided a 70% reduction in the common mode current, a 4% reduction in the size of the geometric footprint, and a 3°C reduction in the maximum temperature over Gen-II.A, thus providing an increase in the overall performance.

NOMENCLATURE

N_p total number of critical input parameters
t time
T temperature
X sensitivity coefficient
β model parameter
σ uncertainty

Subscripts

M measured
N nominal
P predicted
S perturbed (for sensitivity calculations)
β model input parameter
∞ ambient

INTRODUCTION

The design target is a new generation of an Integrated Power Electronics Module (Generation (Gen) II–IPEM), which is packaged using embedded power technology, a hybrid multi chip module (MCM)-based packaging technology [1]. The multiple bare chips of metal oxide semiconductor field effect transistor (MOSFETs) or insulated gate bipolar transistors (IGBTs) are buried in a ceramic frame, and covered by dielectrics with holes on the aluminum pads of the chips. The power devices are interconnected to other circuits by metal deposition. This new package method eliminates wire bonds, which could lead to potential benefits from both the electrical and thermal perspectives. The objective for this research effort was to develop and implement an integrated design strategy to improve the layout design of Gen II–IPEM by reducing the electrical stress, the conduction EMI, and the thermal resistance, while minimizing the geometric footprint.

Parasitic inductance stores energy when current flows through it. When the device needs to be turned off, the energy is released as a voltage spike if no external snubber exists. The spike is a function of the inductance and the current rate, and the current rate becomes larger at higher frequencies. To improve long-term reliability, it is required that the parasitic be small enough to limit the spike. Also the common mode capacitance needs to be reduced in order to meet the EMI standard. Therefore, it is important to calculate the parasitic inductance and the capacitance of the IPEM.

Thermal management is another critical task in the design of power electronic systems. Bar-Cohen [2] noted that the choice of the strategy used for the thermal management of an electronic product has a large impact on the cost, reliability, operating environment and performance of the system. Thus, while thermal control is just one of several enabling packaging technologies, it deserves and must receive special attention. Good thermal design is often required to achieve high reliability, low manufacturing costs, small size, and a predictable development time. The system must be designed to dissipate the maximum amount of power without exceeding the maximum $T_{junction}$ specification, which is 125°C for the materials in this paper. Thus, thermal and flow analyses software tools can be used to identify hot

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spots and other thermally important areas on the IPEM, and assess the thermal impact of proposed design changes, such as in the choice of materials and the geometric layout.

Within the module, heat is transferred primarily by conduction through numerous complex components with different thermo-physical properties and thicknesses [3]. In a recent investigation of package structure optimization, researchers at the Toshiba Corporation [4] studied the rise in the junction to case temperature difference as a function of the thickness of the heat spreader and the distance between the chips. However, the reduction in the thermal contact resistance was large enough to reduce the temperature rise of the heat sink, and therefore, the chip temperature was reduced as the thickness of the copper heat spreader increased. The Motorola Hybrid Power Modules Operations team [5] also studied the thermal characterization of Direct Bonded Copper (DBC) and MMC stacks for power modules. Their results indicated that reducing the ceramic thickness would improve the maximum junction temperature with Aluminum Oxide (Al_2O_3), but not with Aluminum Nitride (AlN).

Meanwhile, researchers also tried to find a way to present experimental and numerical results with describing the uncertainties involved. Thus, Moffat [8] presented a way to describe the uncertainties in experimental results. First, he identified the sources of errors in engineering measurements and the relationship between the error and uncertainty. From there, the intended true value of a measurement was identified through the quantitative estimation of the individual errors. Moffat also presented a technique for numerical executing analyses when computerized data interpretation is involved.

With this basis, the objective of this effort was to develop and implement an integrated electro-thermal design strategy for the next generation of the Gen-II IPEM. This paper is primarily focused on the thermal aspects of the design, while details of the electrical aspects are provided in [6].

INTEGRATED DESIGN STRATEGY

A two step integrated design strategy was employed. First, the parasitic inductance and capacitance of the existing IPEM (identified as Gen-II.A) were analyzed, and then a number of new electrically feasible layout improvements were proposed. The best of these was then selected and named Gen-II.B. The second step involved a detailed thermal parametric study of the Gen-II.B layout to further refine the design. Several factors were investigated, including the type of material and the thickness of the DBC ceramic substrate, and the thickness of the heat spreader. A sensitivity study was then performed to determine the uncertainty of the predicted temperatures at critical locations. The final design, Gen-II.C, was then based on a trade off between electrical, thermal, and practical considerations.

ELECTRICAL AND THERMAL ANALYSIS

Electrical Modeling

The first step of the design methodology began with the development of a numerical model that included critical electrical components of the Gen-II.A design. This model was used to extract the parasitic inductance and determine the capacitance values. Transient simulations and an EMI analysis were then performed to determine the electrical stress of device and the common mode EMI current. Based on these analyses, a number of new layouts were proposed to reduce the geometric footprint of the module, and a parametric study was conducted to determine the effects of the geometric size of the copper trace area and the DBC substrate thickness on the electrical performance. Details of the electrical modeling and analyses are described in [6].

Thermal Modeling

The second step of the design strategy began with a detailed thermal analysis of the Gen-II.A and Gen-II.B IPEMs using a commercial finite element and computational fluid dynamics (CFD) solver, I-DEAS. This involved developing numerical models and carrying out simulations to identify hot spots as well as to predict steady-state temperature distributions within the module. A parametric study was performed to determine the effects of the type of material and the thickness of the ceramic substrate, and the thickness of the heat spreader on the thermal performance of the IPEM. The parameters used in this analysis are shown in Table 1.

All of the simulations in the parametric study were also performed using I-DEAS. Each model included a full 3D IPEM with an optional heat spreader mounted on an aluminum heat sink. A flow channel, with dimensions of 69.5mm (W) x 123.5mm (H) x 325mm (L), was included to provide air flow over the model. An inlet fan with a constant volumetric flow rate of 0.0094 m^3/s was applied at one end of the channel, while the other end of the channel was vented to an ambient temperature of 50°C, as shown in Fig. 1(a). The area of the channel was fixed, resulting in an outlet velocity of 1.1 m/s. The top of the module was assumed to be adiabatic.

Each module had three heat sources: two MOSFET's and a gate driver. The heat losses of the two MOSFET's were measured to be 12W for the outside one (A) and 7W for the innermost one (B). The hybrid gate driver only dissipated 1W, as shown in Fig. 1(b). Due to its relatively low power loss, the gate driver was modeled as a homogeneous ceramic block. Fine grids were used for the heat dissipating surfaces. In addition, all soldered components and interfaces with thermal grease (e.g. at the interface between the heat spreader and the heat sink in Fig. 1(c)) were represented by equivalent thermal resistance values. Within the IPEM model, it was assumed that there was a conduction path from the two heat sources to the copper trace and the surrounding ceramic substrate, from the copper trace to the second DBC ceramic layer, and from the ceramic layer to the bottom copper layer. From there, it was assumed that the major heat flow paths involved conduction from the IPEM module to the (optional) heat spreader, conduction from the heat spreader to the heat sink, and convection from both the heat spreader and the heat sink to the ambient air. Another path of resistance was from the gate driver to the ceramic substrate, from the ceramic substrate to a layer of gel, and from the gel to the DBC layer. The thermal conductivities for all of the materials used in the models are listed in Table 2.

Sensitivity and Uncertainty Analysis

Once the parametric studies were completed, sensitivity and uncertainty studies were performed to determine the predictive uncertainty of various temperatures in the model. The sensitivity of a given parameter refers to how sensitive a given output variable is to changes in that parameter, while the measurement uncertainty of a parameter reflects how accurately the parameter values used in the model are known. Ideally, we would like the parameters with the highest sensitivity to have the lowest uncertainty, and parameters with high uncertainty to have low sensitivity.

A four-step analysis strategy was employed for the uncertainty analysis. First, several critical model input parameters and output variables were identified, and are shown in Fig. 2. The critical input parameters included the power losses of both MOSFETs and all of the interface conditions, including the epoxy, solder, and the thermal grease, and the critical output variables included the junction, gate, and minimum heat sink temperatures, and the average temperature of

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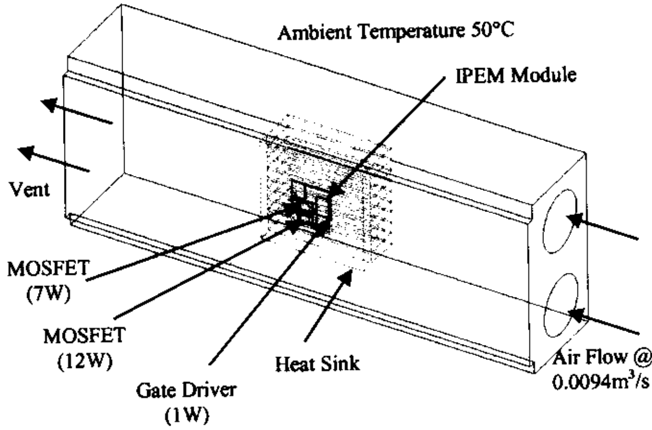
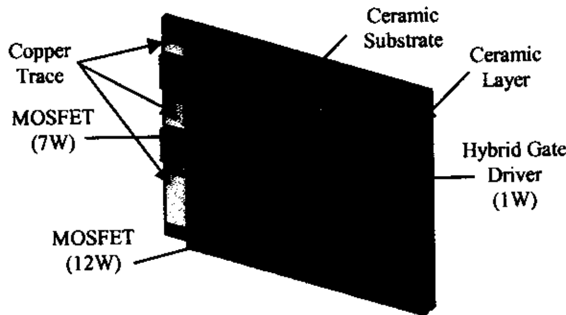
Table 1. Parameters used in Second Step of Thermal Analysis.

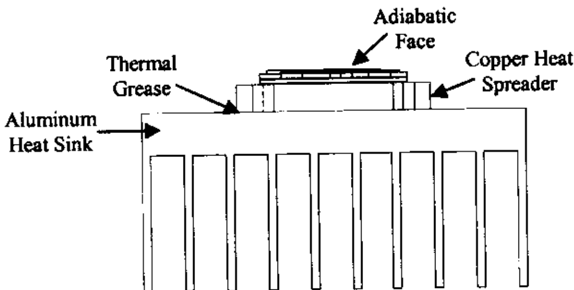
Parameter	Value			
DBC Ceramic Material	Al_2O_3	AlN		
DBC Ceramic Thickness	0.38 mm	0.635 mm	1.02 mm	
Heat Spreader Thickness	0 mm (none)	1 mm	3 mm	5 mm



(a) Boundary Conditions



(b) Details of the IPEM Model



(c) Positioning of Components on Heat Sink

Figure 1. IPEM Model used in all Thermal Analyses.

the module. Since this study focused only on the module itself without concerning the effect of the convection from the heat sink, the fluid flow and convection heat transfer parameters were not considered as the sensitivity parameters. Future study will focus on the optimization of the heat sink and the sensitivity and uncertainty analyses on the

Table 2. Thermal Conductivity Values for Materials used in Thermal IPEM Model.

Material	Thermal Conductivity (W/mK)
Copper	395
Aluminum	164
Ceramic AlN	150
Ceramic Al_2O_3	26
Solder	51
Thermal Grease	1
Silicone Gel	0.2
Epoxy	1.4

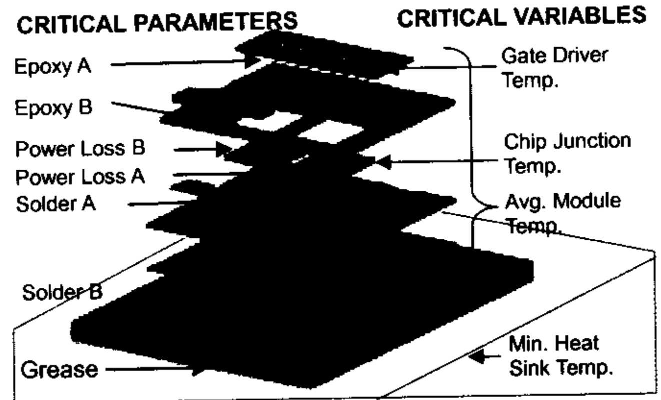


Figure 2. Location of Interest in IPEM for Sensitivity and Uncertainty Analysis.

Table 3. Nominal Values and Measurement Uncertainty of Parameters Used in Sensitivity and Uncertainty Analysis.

Sensitivity Parameter, β_i	Location	Nominal Value, β_{Ni}	Uncertainty, σ_{Mi}
Power Loss A	Outermost MOSFET	12 W	+3 W
Power Loss B	Innermost MOSFET	7 W	+3W
Epoxy A	Between Silicon & Ceramic Substrate	0.51 mm	±0.025 mm
Epoxy B	Between Gate Driver & Ceramic Substrate	0.13 mm	±0.025 mm
Solder A	Between Silicon & DBC Copper Trace	0.13 mm	±0.025 mm
Solder B	Between DBC Copper Base & HS	0.13 mm	±0.025 mm
Thermal Grease	Between Heat Spreader (HS) & Heat Sink	0.13 mm	±0.025 mm

convection heat transfer parameters. The second step involved the determination of the measurement uncertainty for each of these parameters. These measurement uncertainties were estimated measurement errors in which the approximations were based on the experience and expertise of the power electronics packaging group in Virginia Tech. These values are shown in Table 3. The third step involved the determination of the sensitivity of each input parameter. Finally, the overall prediction uncertainties of the critical output variables were determined from the sensitivities and measurement uncertainties of each of the critical input parameters.

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The sensitivity coefficient for each parameter was defined as a dimensionless term, X_i^+ :

$$X_i^+ = \frac{\delta T^+}{\delta \beta^+} = \frac{\Delta T^+}{\Delta \beta_{Si}^+} \quad (1)$$

The non-dimensional temperature, ΔT^+, is defined by

$$\Delta T^+ = \left| \frac{T_N(\beta_{Ni}) - T_S(\beta_{Si})}{T_N(\beta_{Ni}) - T_\infty} \right|, \quad (2)$$

where T_∞ is the ambient temperature, and $T_N(\beta_{Ni})$ and $T_S(\beta_{Si})$ are the respective predicted temperatures for each parameter using β_{Ni} and β_{Si}, where β_{Si} is the perturbed value and β_{Ni} is the nominal value of the sensitivity parameter, and

$$\beta_{Si} = \beta_{Ni} + 0.01 \cdot \beta_{Ni}. \quad (3)$$

Note that $T_N(\beta_{Ni})$ is also referred to as the nominal temperature. Finally, the non-dimensional sensitivity difference, $\Delta(\beta_S)_i^+$, is defined as

$$\Delta \beta_{Si}^+ = \left| \frac{\Delta \beta_{Si}}{\beta_{Ni}} \right|, \quad (4)$$

where $\Delta\beta_{Si}$ is the 1% variation of the nominal value β_{Ni}; the nominal values used are also shown in Table 3.

The predictive uncertainties for each parameter, σ_{Pi}, were then determined from the sensitivities and measurement uncertainties, σ_{Mi}, as follows [8]:

$$\sigma_{Pi} = X_i^+ \cdot \sigma_{Mi}, \quad (5)$$

where X_i^+ is the sensitivity coefficient defined in Eq. (1). The overall uncertainty for the jth output variable, σ_j, was then defined as

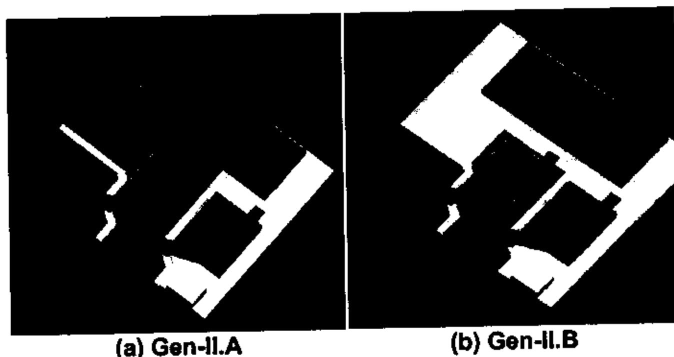
$$\sigma_j = \sqrt{\sum_{i=1}^{N_P} (\sigma_{Pi})^2} = \sqrt{\sum_{i=1}^{N_P} (X_i^+ \cdot \sigma_{Mi})^2}, \quad (6)$$

where N_P is the number of critical input parameters.

RESULTS AND DISCUSSION

Results of the Electrical Analysis

A summary of the results from the electrical analysis is provided here; details can be found in [6]. As a result of the parasitic inductance and capacitance analyses, a number of new layouts were proposed to reduce the geometric footprint of the module and improve electrical performance. The best of these resulted in Gen-II.B, and included a substantial reduction (by a factor of ~3) in the copper trace area and a 4 percent reduction in the geometric footprint, as shown in Fig. 3. In addition, a bus capacitor was added to reduce the voltage overshoot of device during switching period.



(a) Gen-II.A (b) Gen-II.B

Figure 3. Initial (Gen-II.A) and Modified (Gen-II.B) IPEM Model from Electrical Optimization with Reduction in Cooper Trace Area. (*Top ceramic layer not shown.*)

The effects of the smaller copper trace area and the DBC ceramic substrate thickness on the electrical performance were then evaluated. Both reducing the trace area and increasing the ceramic layer thickness were found to substantially increase electrical performance, while the choice of material (AlN or Al_2O_3) had only a moderate effect. Hence, since thermal resistance increases with thickness, a trade-off was expected between electrical and thermal performance.

Results from the Thermal Analysis

A thermal analysis was first conducted on the Gen-II.A and B IPEMs to determine the overall temperature distributions and the peak temperatures, as shown in Fig. 4 and Table 4. The maximum temperature in both cases was located at the outer MOSFET. The Gen-II.B design resulted in a maximum temperature increase of almost 4°C and an overall average increase of almost 3°C over the Gen-II.A design. Hence, although the reduction in the size of the footprint and the copper trace area in Gen-II.B increased electrical performance as noted previously, it decreased thermal performance.

Thus, the second phase of the thermal analysis involved a parametric study to identify critical factors to improve the thermal performance of Gen-II.B. Eight cases based on the Gen-II.B design were studied, as shown in Table 4. The maximum temperatures in the MOSFETs and the gate driver and the overall average temperature are provided for each case; all predicted satisfactory operation under the 125°C temperature limit.

The DBC ceramic layer was first investigated. The effect of the ceramic material was moderate: the use of AlN (Case 1) instead of Al_2O_3 reduced the junction temperature by only 1.5°C, despite the large change in thermal conductivity shown in Table 2. This is due to its relatively low contribution to the overall thermal resistance of the IPEM. The thickness of the layer was then varied from 0.635 mm (Gen-II.B) to 0.38 mm (Case 2) and to 1.02 mm (Case 3). The electrical performance was shown to increase as the ceramic layer increased [6]; however, from Table 4 and Fig. 5, this variation had little effect on the thermal performance as all results were within 0.2°C.

The effect of adding a copper heat spreader on the module was then analyzed, as shown by Cases 4 - 6 in Table 4 and Fig. 5. The addition of the heat spreader was most significant, as the maximum MOSFET and average temperatures dropped up to 7°C – below the Gen-II.A values. Note that the lower Cu layer was soldered onto the heat spreader, and then the heat spreader was placed on the heat sink with thermal grease. In the case without the heat spreader, thermal grease was used between the module and the heat sink. The effect of the thickness of the heat spreader was moderate as shown in Fig. 6. The MOSFET temperature increased 1°C as the thickness increased from 1 to 5 mm. These results agree with those presented by the Toshiba Corporation [4]. The temperature rise here is small since the material was copper. As a result, the heat spreader hindered the heat transfer slightly due to the added resistance layer, but it promoted heat transfer even more by providing a large conductive surface to dissipate heat. Case 7 shows the effect of the material choice for the ceramic layer with the 5 mm heat spreader. Although this case provided the best thermal performance, the effect was moderate, as the AlN ceramic resulted in a 1.4°C decrease in the MOSFET temperature.

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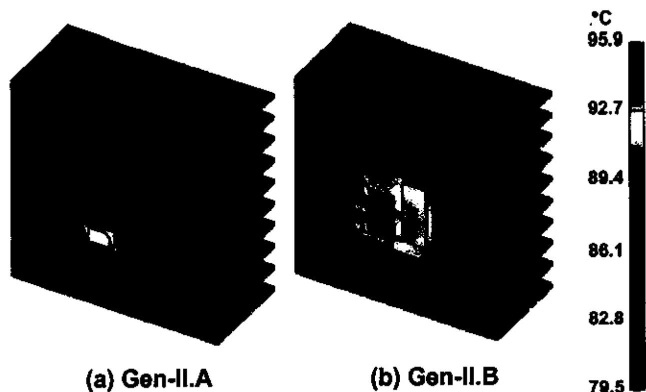

Figure 4. Steady-State Temperature Distributions Models.

Table 4. Summary of Results from the Thermal Simulations and the Parametric Study.

IPEM Model	IPEM Size (mm^2)	Ceramic Mat'ls	DBC Ceramic Thickness (mm)	Heat Spreader (HS) Thickness (mm)	Max. MOSFET Temp. (°C)	Max. Gate Temp. (°C)	Avg. Module Temp. (°C)
Base Models							
Gen-II.A	x[1]	Al_2O_3	0.635	NA	92.2	87.4	88.1
Gen-II.B	y[2]	Al_2O_3	0.635	NA	95.9	93.2	90.7
Gen-II.B Modifications							
Case 1 (AlN)	y[2]	AlN	0.635	NA	94.4	92.2	90.1
Case 2 (0.38 mm DBC)	y[2]	Al_2O_3	0.38	NA	95.9	93.1	90.6
Case 3 (1.02 mm DBC)	y[2]	Al_2O_3	1.02	NA	96.0	93.3	90.8
Case 4 (1 mm HS)	y[2]	Al_2O_3	0.635	1	88.7	87.7	84.2
Case 5 (3 mm HS)	y[2]	Al_2O_3	0.635	3	89.3	88.7	85.8
Case 6 (5 mm HS)	y[2]	Al_2O_3	0.635	5	89.7	89.6	86.2
Case 7 (AlN_3+ 5 mm HS)	y[2]	AlN	0.635	5	88.3	88.4	85.6
Case 8 (5 mm HS +Centered)	y[2]	Al_2O_3	0.635	5	89.7	89.8	86.5

[1] x =26.9 mm × 30.0 mm;
[2] y = 28. 5 mm × 27.3 mm

Case 8 evolved through an analysis of Case 6 (Fig. 7(a)). In looking at the temperature distribution on the heat spreader in Case 6 (Fig. 7(c)), it was evident that the heat flow was asymmetric, and this prompted a modification to increase the heat spreader's effectiveness. The heat spreader was centered under the primary heat source, resulting in Case 8. Although the resulting temperature distribution is more symmetrical, the MOSFET temperature was virtually unchanged and the gate driver temperature increased slightly (see Figs. 7(a,b) and Table 4). (Note, however that both are significantly lower than those for Gen-II.B in Fig. 4(b).) The temperature distribution on the heat spreader for Case 8 (Fig. 7(d)) revealed that although it appeared that the heat was being effectively distributed from the MOSFETs, there was little evidence that the same was true for the gate driver. Thus, even though power loss of the gate driver was only 1W, it became the limiting factor in the thermal analysis, indicating a need for future detailed analyses of the gate driver.

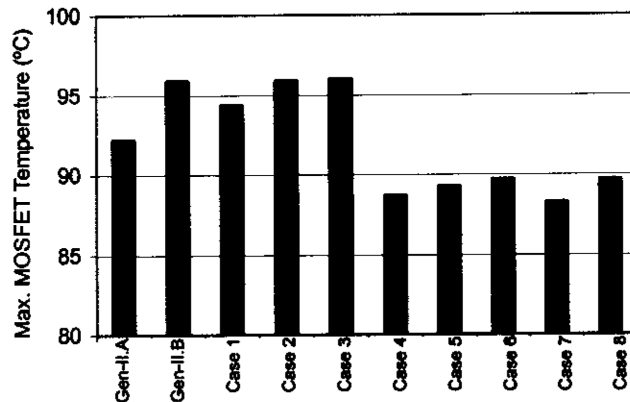

Figure 5. Maximum MOSFET Temperature for Gen-II.A, Gen-II.B, and 8 Cases from Parametric Study.

Sensitivity and Uncertainty Analysis

In any modeling analyses, it is important to understand the uncertainty in the predicted temperatures. The Gen-II.B IPEM with a 5 mm thick heat spreader (Case 5) was chosen as the model for all of the uncertainty analyses. Sensitivity coefficients were calculated using Eq. (1) for each of the critical input parameters for each of the critical output variables; results are shown in Fig. 8. The most sensitive parameter is the thickness of Solder B, which is between the DBC copper layer and the heat spreader, followed by Power Loss A (12W). The sensitivity of the solder thickness at the chip is well over three times higher than that of the other parameters. This indicates the importance of using a highly conductive material (i.e., solder rather than thermal grease) at this interface. The variation in the other parameters is considered to be insignificant in all cases.

The predicted uncertainty of each parameter was then calculated from Eq. (5) using the sensitivities in Fig. 8 and the measurement uncertainties in Table 3. The results are shown in Fig. 9. Again, the thickness of Solder B, between the DBC copper layer and the heat spreader, contributed the highest uncertainty in the IPEM model.

The overall uncertainty was then calculated using Eq. (6) for each of the critical output variables, as shown in Fig. 10. The result shows that the junction temperature has the most uncertainty followed by the average temperature of IPEM. The minimum heat sink temperature has the least uncertainty among the four investigated temperatures. Based on the results we obtained, we can characterize the uncertainty associated with the thermal model.

Thus, from this analysis, the predicted chip junction temperature has the highest uncertainty at 8°C. If one takes in to account this uncertainty in the predicted values, all temperatures (in Table 4) are still less than the 125°C maximum limit. Most importantly, this analysis emphasizes the importance of developing methodologies to accurately estimate power losses and interface conditions.

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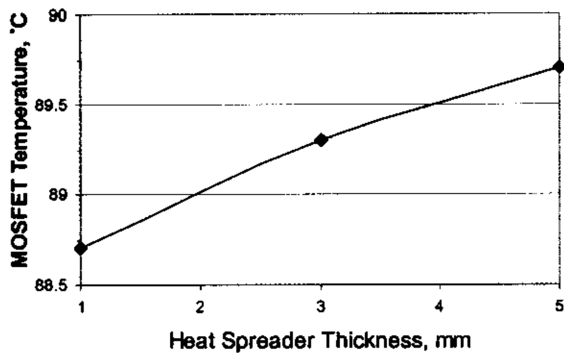

Figure 6. Effect of Heat Spreader Thickness on Maximum Temperature of Gen-II IPEM.

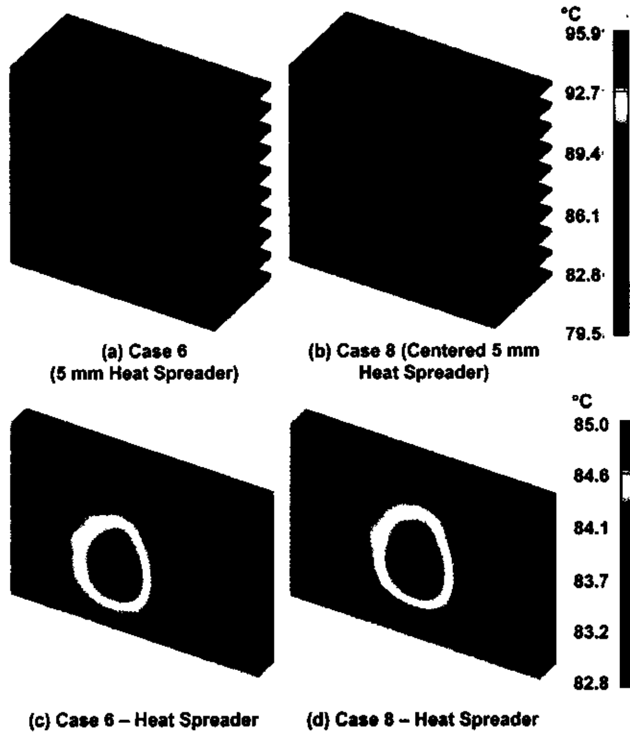

Figure 7. Steady-State Temperature Distributions for Cases 6 and 8.

Design Selection

In selecting the best design, we realize that there are trade-offs between the electrical, thermal, and practical considerations. Fig. 11 shows the trade-offs for three different thicknesses of DBC ceramic in which these selected thicknesses are the currently available thicknesses from manufacturers. With regards to the choice of the ceramic layer, we can see from Fig. 11 that electrical performance increases and thermal performance decreases as the thickness increases, although the effect on electrical performance is significantly greater than that for the thermal performance. In addition, the cost of a 1.02 mm thick DBC ceramic is 17% much more expensive than a 0.635 mm thick DBC ceramic. Thus, based on this trade-off and cost considerations, we selected the optimum thickness at 0.635 mm. In either case, the AlN ceramic material proved to be beneficial, but was not chosen due to its comparably high cost – a practical consideration.

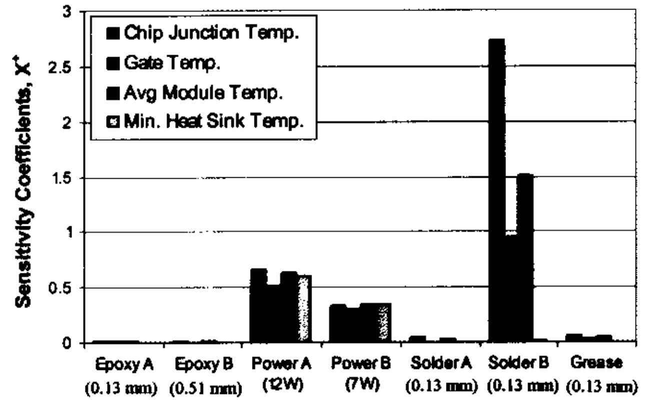

Figure 8. Sensitivity for Each Critical Parameter on each of the Critical Output Variables.

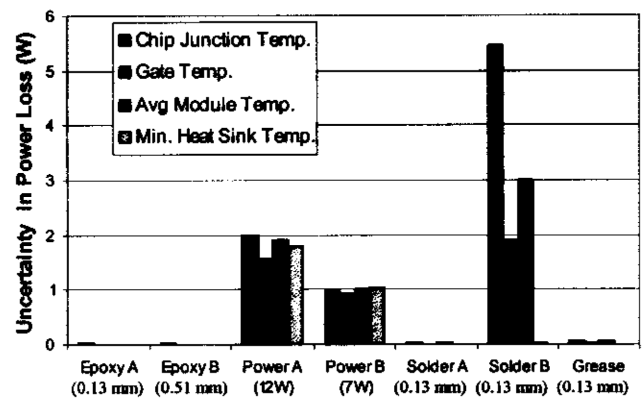

Figure 9. Sensitivity-uncertainty for Each Critical Parameter on each of the Critical Output Variables.

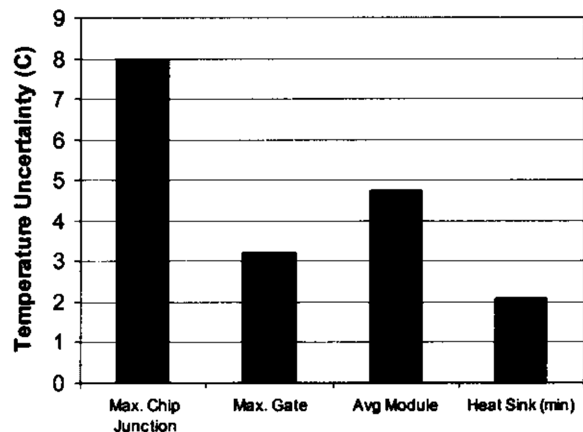

Figure 10. Overall Uncertainty for Each Critical Output Variable.

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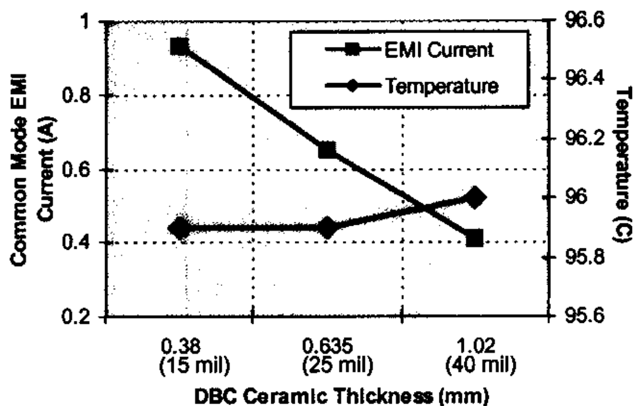

Figure 11. Trade-offs between electrical and thermal performance for different DBC Ceramic Thicknesses.

Table 5. Specifications for Final Design.

IPEM Model	IPEM Size (mm^2)	Ceramic Mat'l	DBC Ceramic Thickness (mm)	Heat Spreader (HS) Thickness (mm)
Gen-II.A	26.9 × 30.0	Al_2O_3	0.635	NA
Gen-II.B	28. 5 × 27.3	Al_2O_3	0.635	NA
Gen-II.C	28. 5 × 27.3	Al_2O_3	0.635	3

Furthermore, from Table 4 and Fig. 5, a 1 mm thick copper heat spreader would provide the best thermal performance. However, structural stability is an important factor too. Because of this and since the loss in thermal performance due to the increased thickness of the heat spreader was small, a 3 mm heat spreader was selected for the final design. Thus, the final design - Gen-II.C - consisted of the following modifications to the Gen-II.B design: a 0.635 mm Al_2O_3 DBC ceramic layer with a 3 mm heat spreader, as shown in Table 5.

SUMMARY AND CONCLUSIONS

A two step integrated design strategy was employed to improve the thermal and electrical performance of an IPEM design. The original design, Gen-II.A, consisted of 1) an IPEM module with a 26.9 mm x 30.0 mm foot print and an almost equivalent copper trace area, 2) a 0.635 mm Al_2O_3 ceramic substrate layer, and 3) no heat spreader. The final design, named Gen-II.C, consisted of 1) an IPEM module with a 4% and 30% reduction in the foot print and copper trace, respectively, and an added bus capacitor, 2) a 0.635 mm Al_2O_3 ceramic substrate layer, and 3) a 3 mm heat spreader.

From the electrical perspective, a bus capacitor was added to reduce the voltage overshoot of semiconductor device, and the reduction in copper trace area reduced the O-to-Ground capacitance to 30% of the Gen-II.A value.

The thermal analysis demonstrated that the choice of material and thickness of the DBC ceramic layer had only a moderate effect on the thermal performance. However, if the costs could be justified, AlN would be a better ceramic material choice than the Al_2O_3, due to its higher thermal conductivity. The addition of the copper heat spreader had a significant effect on the thermal performance, as the presence of a 1 mm layer decreased the maximum temperature of Gen-II.B by 7°C. The choice of a 3 mm layer was due to structural considerations. In addition, it was found that the heat dissipation from the gate driver is poor, and should be examined more carefully in the future. It should be emphasized that, due to the complexity of the multi-source interactions, these observations could have not been easily visualized without the detailed 3D thermal analysis.

The sensitivity analysis demonstrated the importance of accurate input parameters – particularly for the most sensitive parameters. More accurate methodologies are needed to estimate the interface conditions and the power losses in particular.

Thus, in conclusion, the two step integrated design strategy was successfully used to redesign the existing Gen-II.A IPEM. The final design, Gen-II.C, provided a 70% reduction in the common mode current, a 4% reduction in the size of the geometric footprint, and a 3°C reduction in the maximum temperature over Gen-II.A, thus providing an increase in the overall performance.

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